1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB

Pansy Build - 08/10/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		394758	ENGINEERING RELEASE		08/10/05

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3 3	Power Block Diagram	N/A N/A
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5 5	Functional / ICT Test	N/A N/A
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30 30	Memory Active Termination	(MASTER) (MASTER)
31 31	Memory Vtt Supply	(MASTER) (MASTER)
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57 76	5V / 1.5V Power Supply	(MASTER) (MASTER)
58 77	2.5V & 1.2V Regulators	(MASTER) (MASTER)
59 78	1.8V Supply	(MASTER) (MASTER)
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69 88	GPU Straps	(MASTER) (MASTER)
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76 103	M1 Net Properties	(MASTER) (MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 10 08:42:29 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 03

SHT 1 OF 103

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8 7 6 5 4 3 2 1

D C B A

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	2	103

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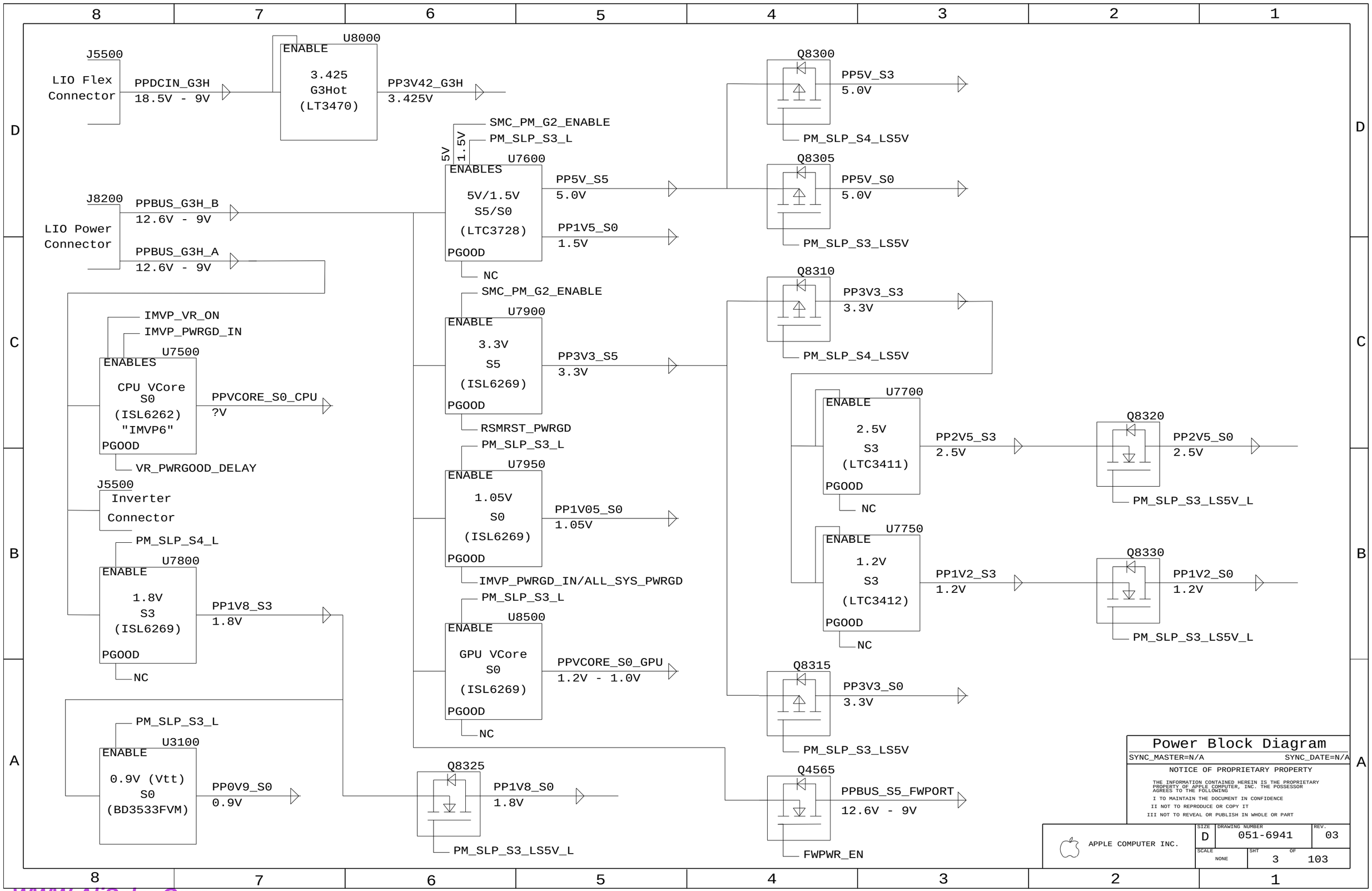

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BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU

BOM GROUP	BOM OPTIONS
M1_COMMON1	CAMERA_S3,CPUCORE_2PIN,GPU_BB_CTL,GPUTHM_A_GPU,INVERTER_BUF,KBDLED_HAS,LCD_CTL_GPU
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,PROTO_ONLY,USB_C_OC_PU,USB_D_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-1175	128S0074	C0935,C0950,C0952,C0953,C0954,C1900	470uF,2.5V,7mOhm	

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	4	103

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Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 76
TRUE	FSB_ADS_L	7 12 76
TRUE	FSB_ADSTB_L<1..0>	7 12 76
TRUE	FSB_BNR_L	7 12 76
TRUE	FSB_BREQ0_L	7 12 76
TRUE	FSB_D_L<63..0>	7 12 76
TRUE	FSB_DBSY_L	7 12 76
TRUE	FSB_DINV_L<3..0>	7 12 76
TRUE	FSB_DRDY_L	7 12 76
TRUE	FSB_DSTBN_L<3..0>	7 12 76
TRUE	FSB_DSTBP_L<3..0>	7 12 76
TRUE	FSB_HIT_L	7 12 76
TRUE	FSB_HITM_L	7 12 76
TRUE	FSB_LOCK_L	7 12 76
TRUE	FSB_REQ_L<4..0>	7 12 76

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 47 48
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S3_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 76
TRUE	ACZ_SDATAOUT	21 44 76
TRUE	ACZ_BITCLK	21 44 76
TRUE	ACZ_RST_L	21 44 76
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_PS_ON	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 76
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUSA_G3H_LIO_CONN	62 63
TRUE	=PPBUSB_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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NC_CPU_A32_L — TP_CPU_A32_L (7)
NC_CPU_A33_L — TP_CPU_A33_L (7)
NC_CPU_A34_L — TP_CPU_A34_L (7)
NC_CPU_A35_L — TP_CPU_A35_L (7)
NC_CPU_A36_L — TP_CPU_A36_L (7)
NC_CPU_A37_L — TP_CPU_A37_L (7)
NC_CPU_A38_L — TP_CPU_A38_L (7)
NC_CPU_A39_L — TP_CPU_A39_L (7)
NC_CPU_APM0_L — TP_CPU_APM0_L (7)
NC_CPU_APM1_L — TP_CPU_APM1_L (7)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
NC_CPU_HFPLL — TP_CPU_HFPLL (7)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
TP_NB_CFG<6> — NB_CFG<6> (14)
TP_NB_CFG<8> — NB_CFG<8> (14)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
TP_NB_CFG<17> — NB_CFG<17> (14)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)

TP_SB_SUS_CLK — SUS_CLK_SB (23)

NC_ENET_CTRL12 — ENET_CTRL12 (37)
NC_ENET_CTRL25 — ENET_CTRL25 (37)

NC_FWPWR_PWRON — =FWPWR_PWRON (40)

FW_PC0 (39)

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (43) — USB2_RT_P — USB_A_P (22)
=USB2_RT_N (43) — USB2_RT_N — USB_A_N (22)
=RTUSB_OC_L (43) — RTUSB_OC_L — USB_A_OC_L (22)

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P (44 5) — USB2_MINI_P — USB_B_P (22)
=USB2_MINI_N (44 5) — USB2_MINI_N — USB_B_N (22)
UNUSED_USB_B_OC_L — USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (44 5) — USB2_LT_P — USB_C_P (22)
=USB2_LT_N (44 5) — USB2_LT_N — USB_C_N (22)
LTUSB_OC_L (44 5) — USB_C_OC_L (22)

USB Port "D" = Camera

=USB2_CAMERA_P (42) — USB2_CAMERA_P — USB_D_P (22)
=USB2_CAMERA_N (42) — USB2_CAMERA_N — USB_D_N (22)
UNUSED_USB_D_OC_L — USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (44 5) — USB2_EXCARD_P — USB_E_P (22)
=USB2_EXCARD_N (44 5) — USB2_EXCARD_N — USB_E_N (22)
EXCARD_OC_L (47 44 5) — USB_E_OC_L (22)

USB Port "F" = Unused

TP_USBP_F — USB_F_P (22)
TP_USBN_F — USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (42) — USB_BT_P — USB_G_P (22)
=USB_BT_N (42) — USB_BT_N — USB_G_N (22)

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P (42) — USB_TRACKPAD_P — USB_H_P (22)
=USB_TRACKPAD_N (42) — USB_TRACKPAD_N — USB_H_N (22)

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI2 (75)
=GND_CHASSIS_DVI3 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI1 (75)
=GND_CHASSIS_DVI4 (75)
=GND_CHASSIS_ENET (38)
=GND_CHASSIS_FW_EMI (41)
=GND_CHASSIS_FW_PORT1 (41)
=GND_CHASSIS_RTUSB (43)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1 — GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_LCD1 (74)
=GND_CHASSIS_LCD2 (74)
=GND_CHASSIS_LCD3 (74)
=GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1 — GND_CHASSIS_INVERTER
2
3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_INVERTER (74)

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	6	103

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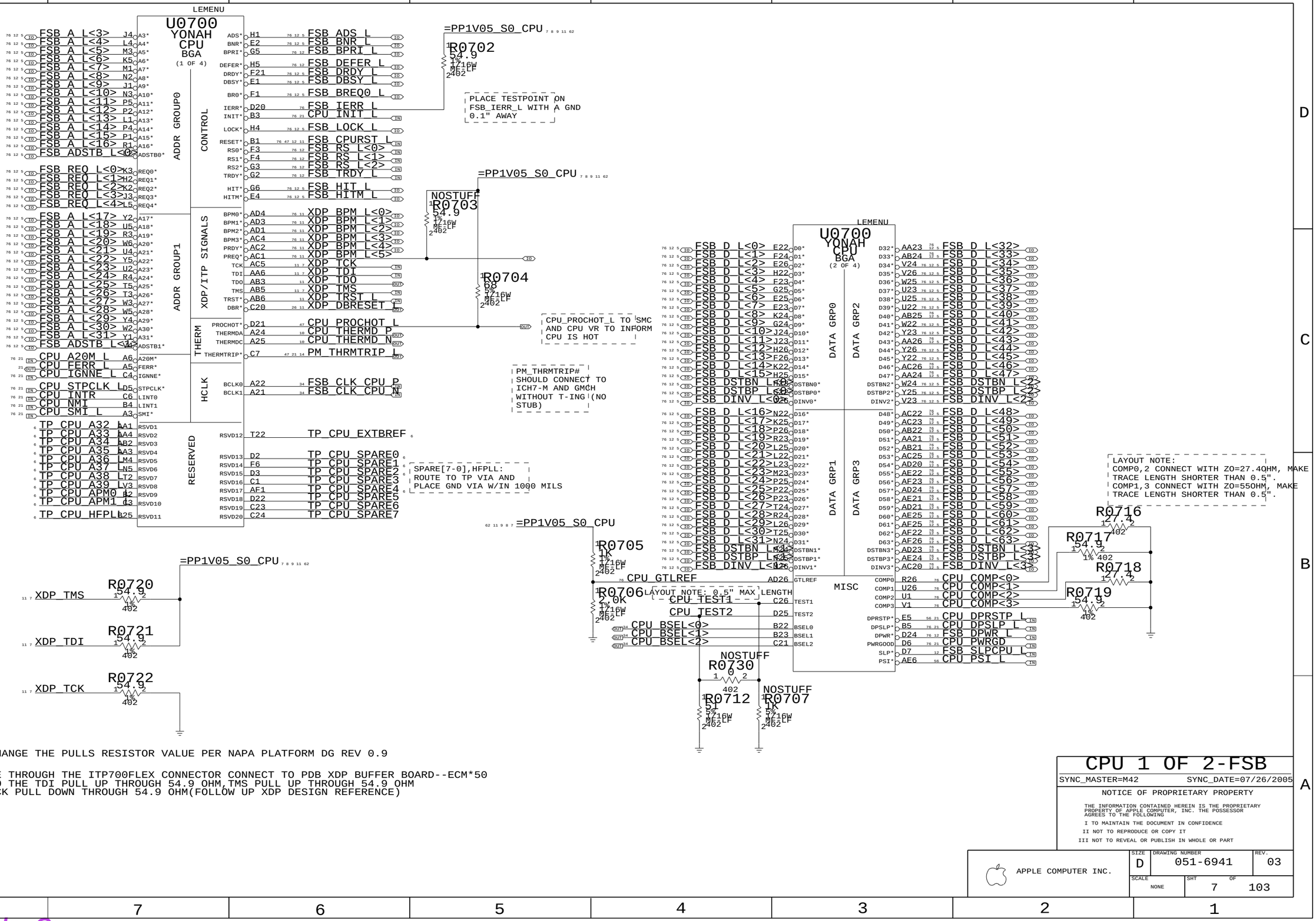

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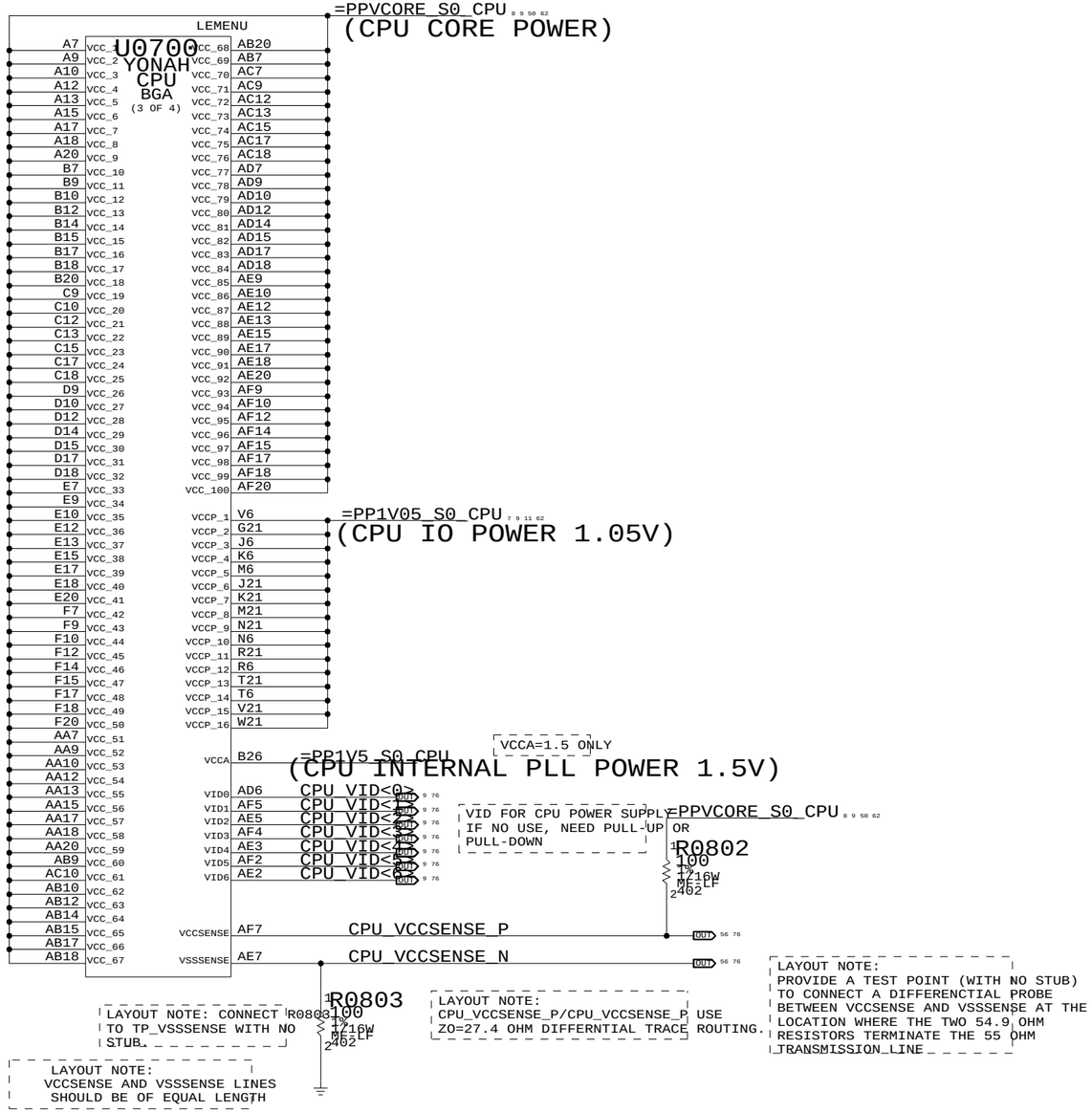

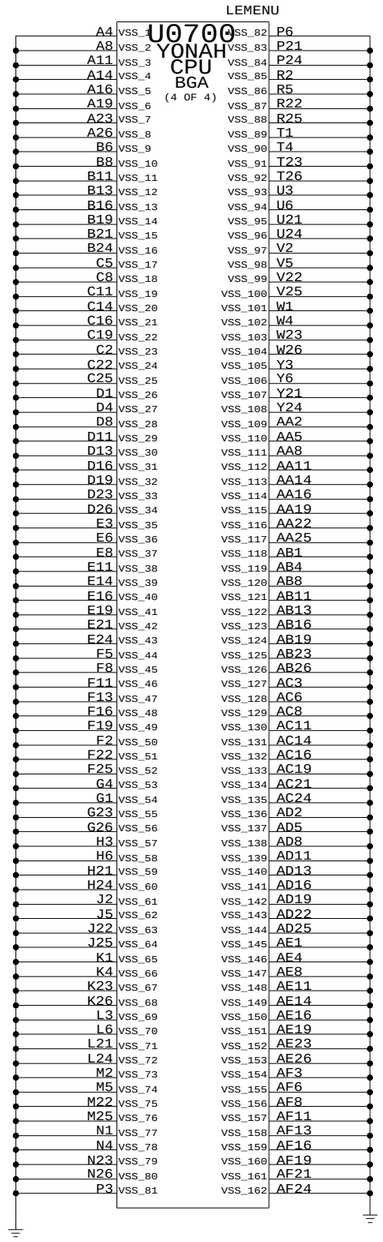

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M42 SYNC_DATE=07/26/2005

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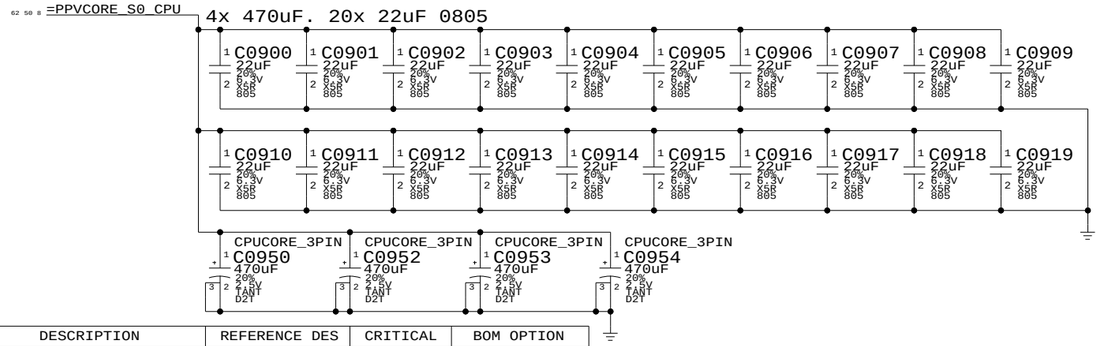
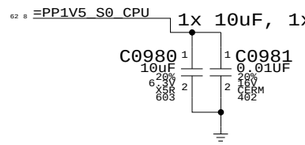
CPU VCORE HF AND BULK DECOUPLING



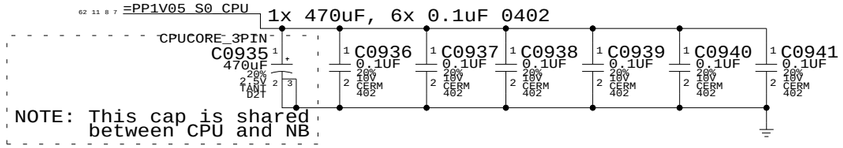
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	4	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0950,C0952,C0953,C0954	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling

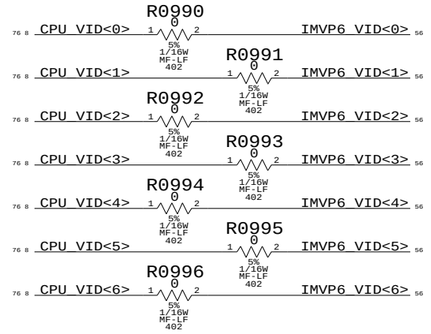

62 11 8 7 =PP1V05_S0_CPU
1x 470uF, 6x 0.1uF 0402
CPUCORE_3PIN
C0935 470uF 20% 2.5V TANT D2T
C0936 C0937 C0938 C0939 C0940 C0941
0.1UF 20% 10V CERM 402
NOTE: This cap is shared between CPU and NB

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0935	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID

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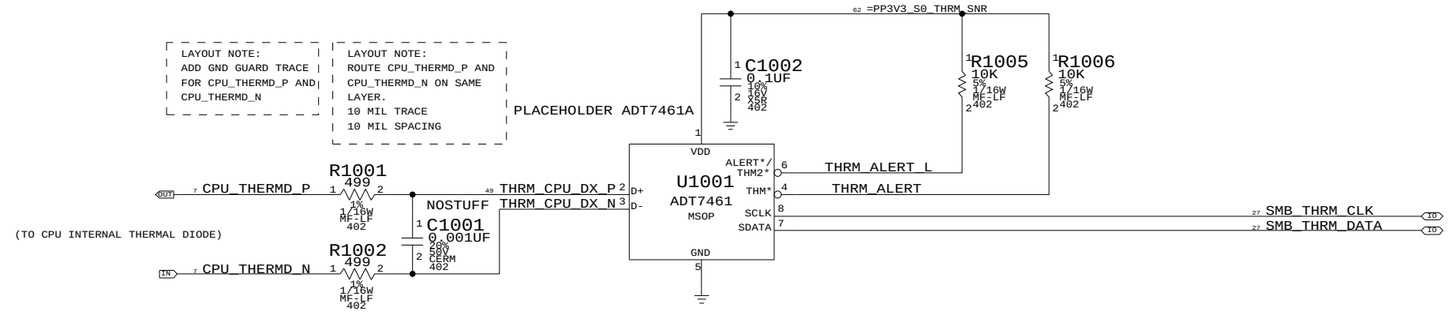
CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

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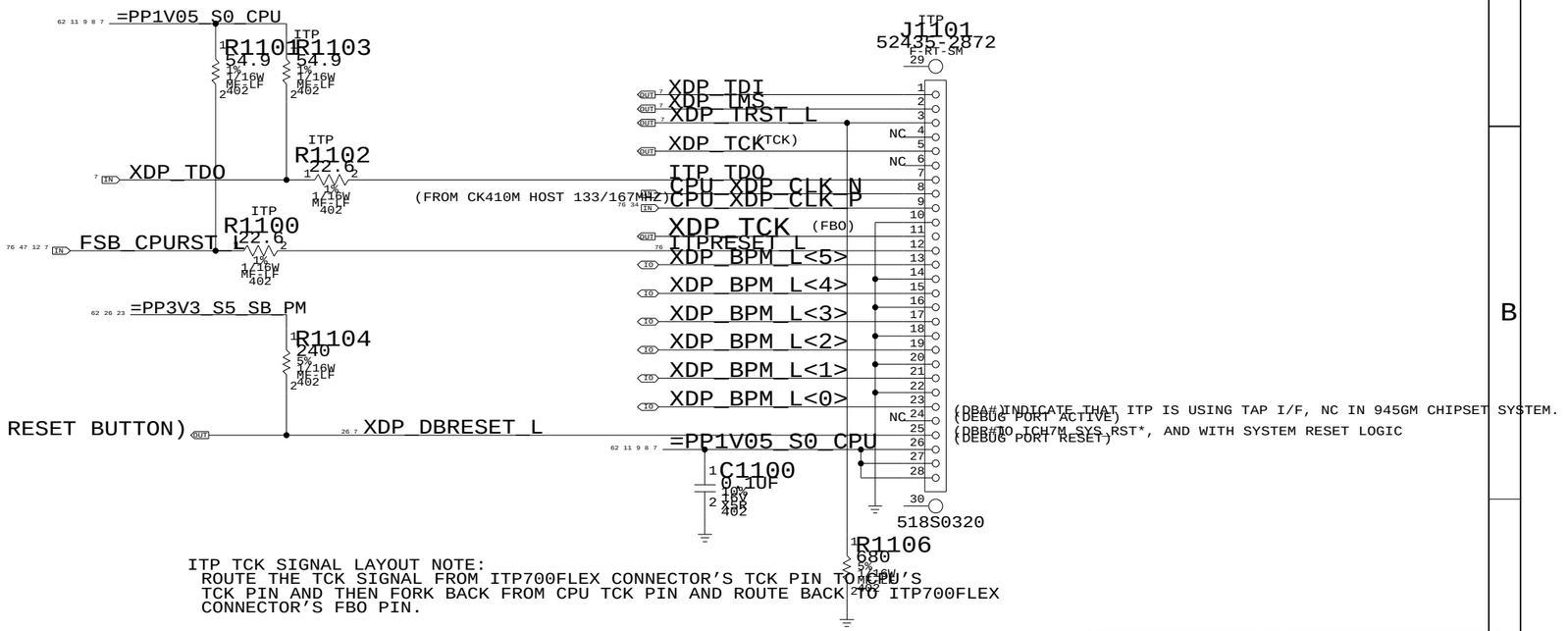
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=07/26/2005

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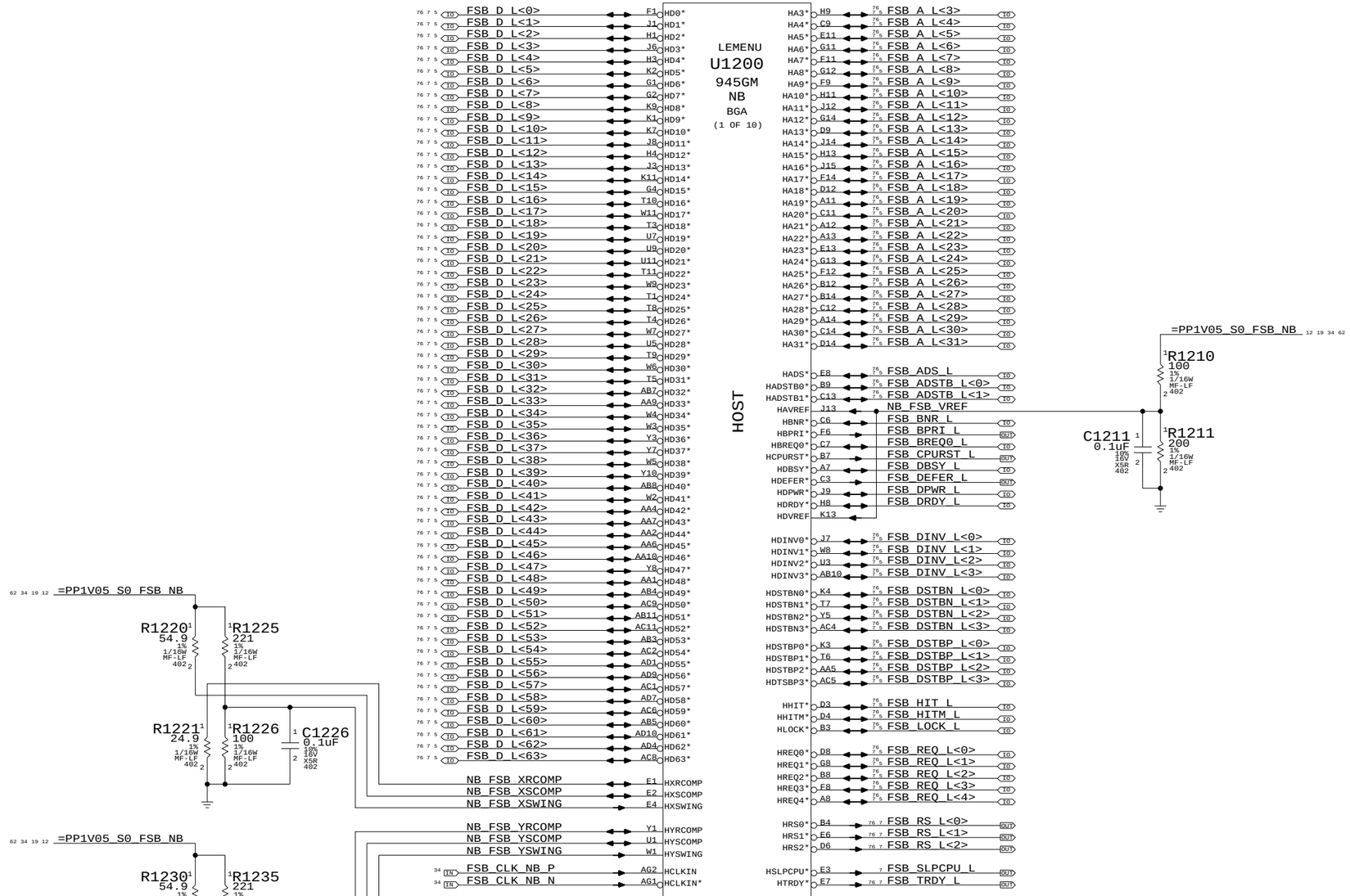

NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

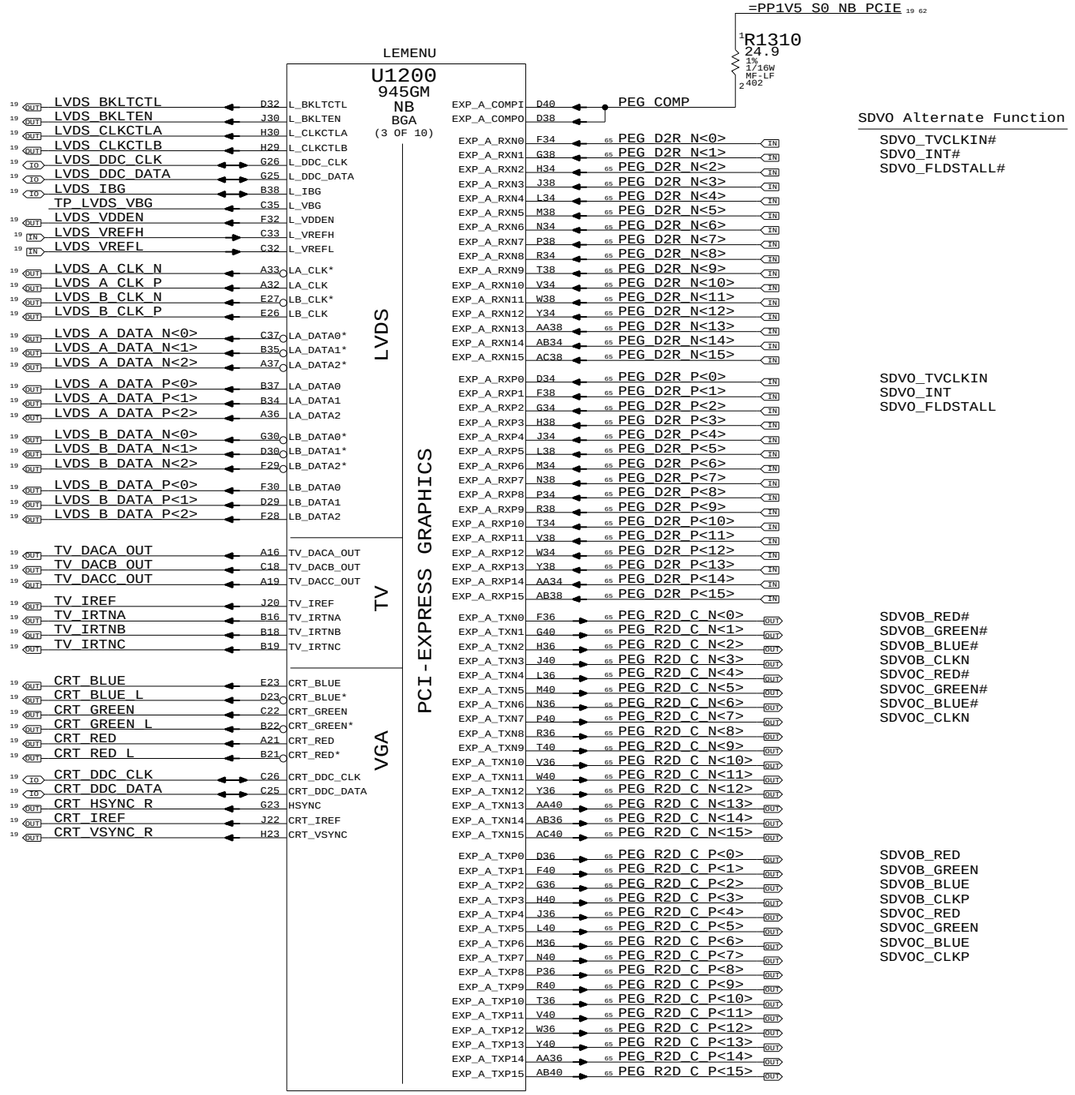
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

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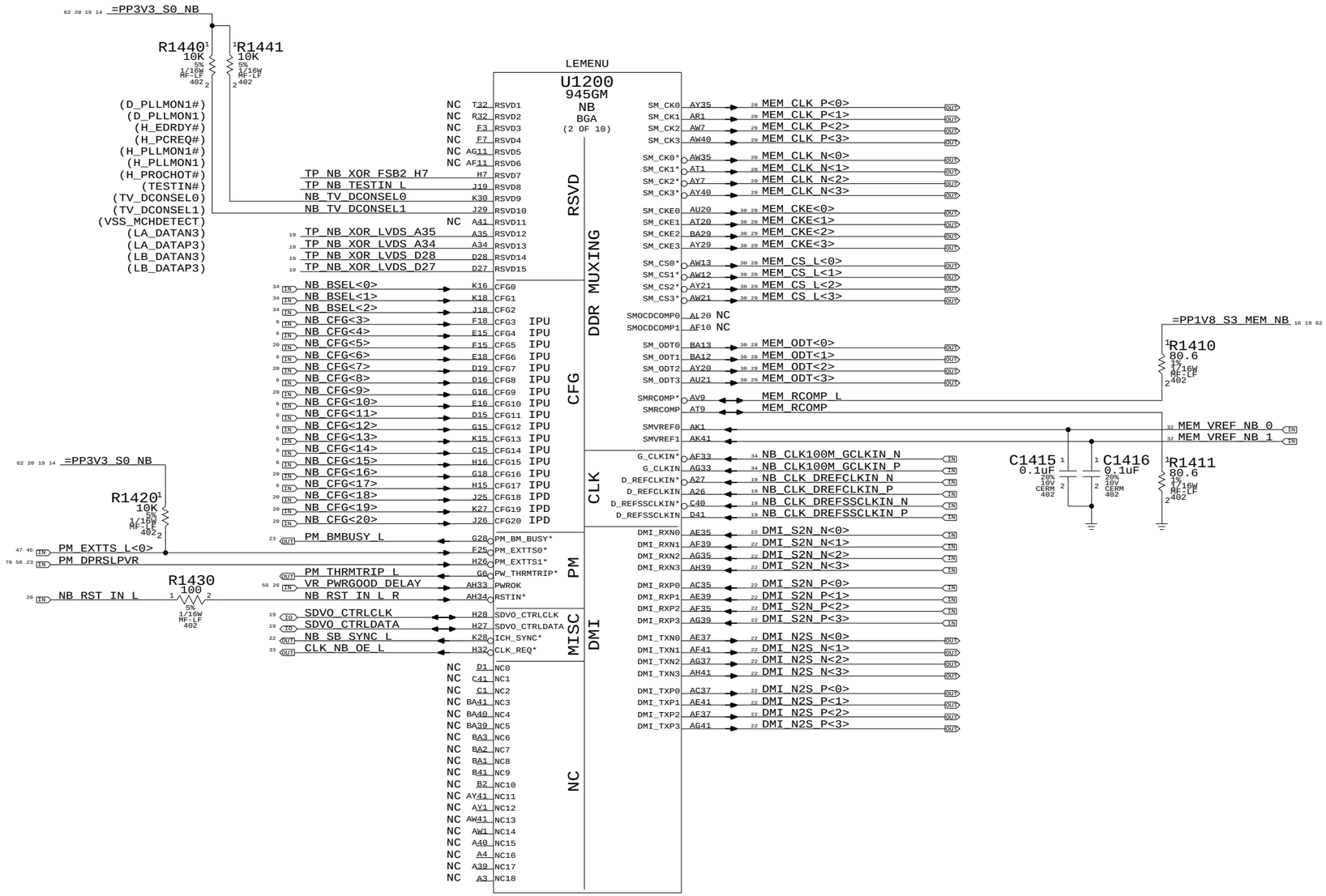

NB Misc Interfaces

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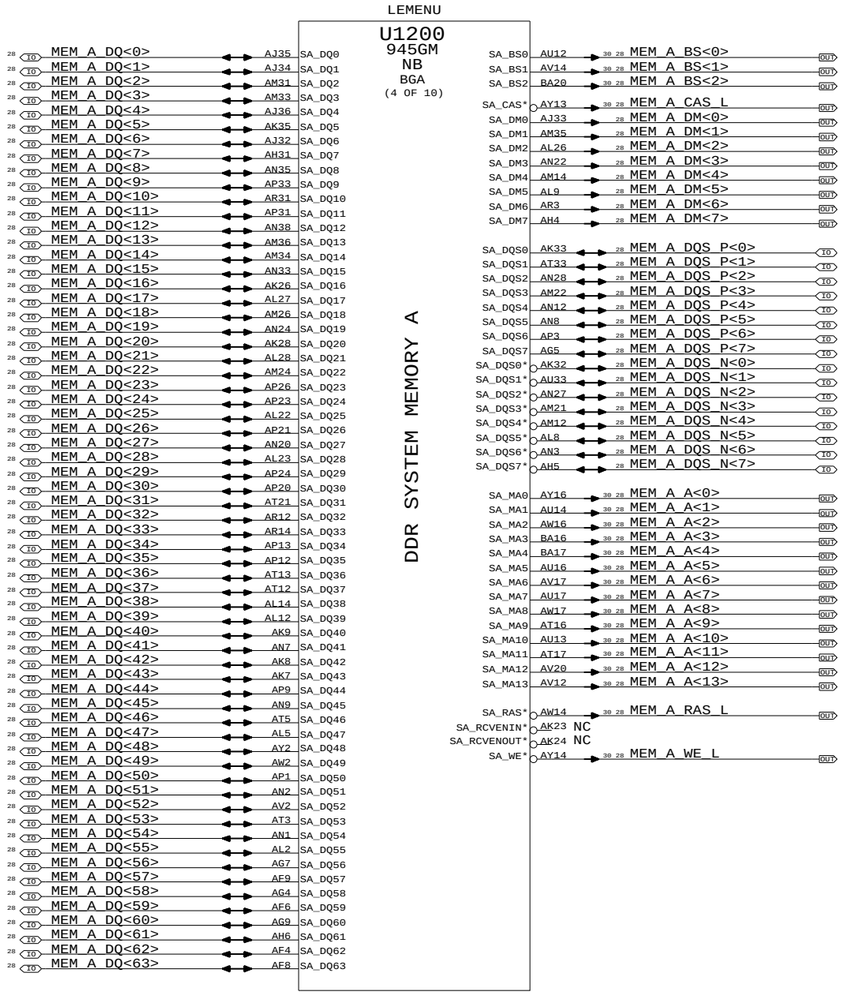

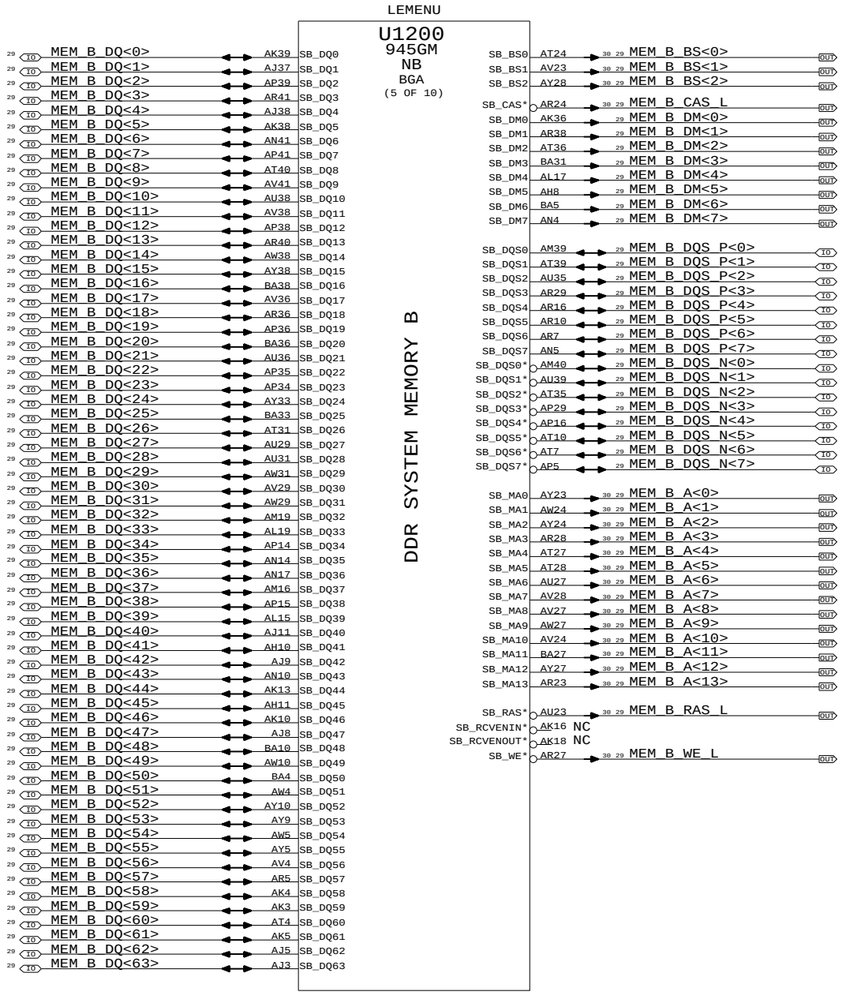

NB DDR2 Interfaces

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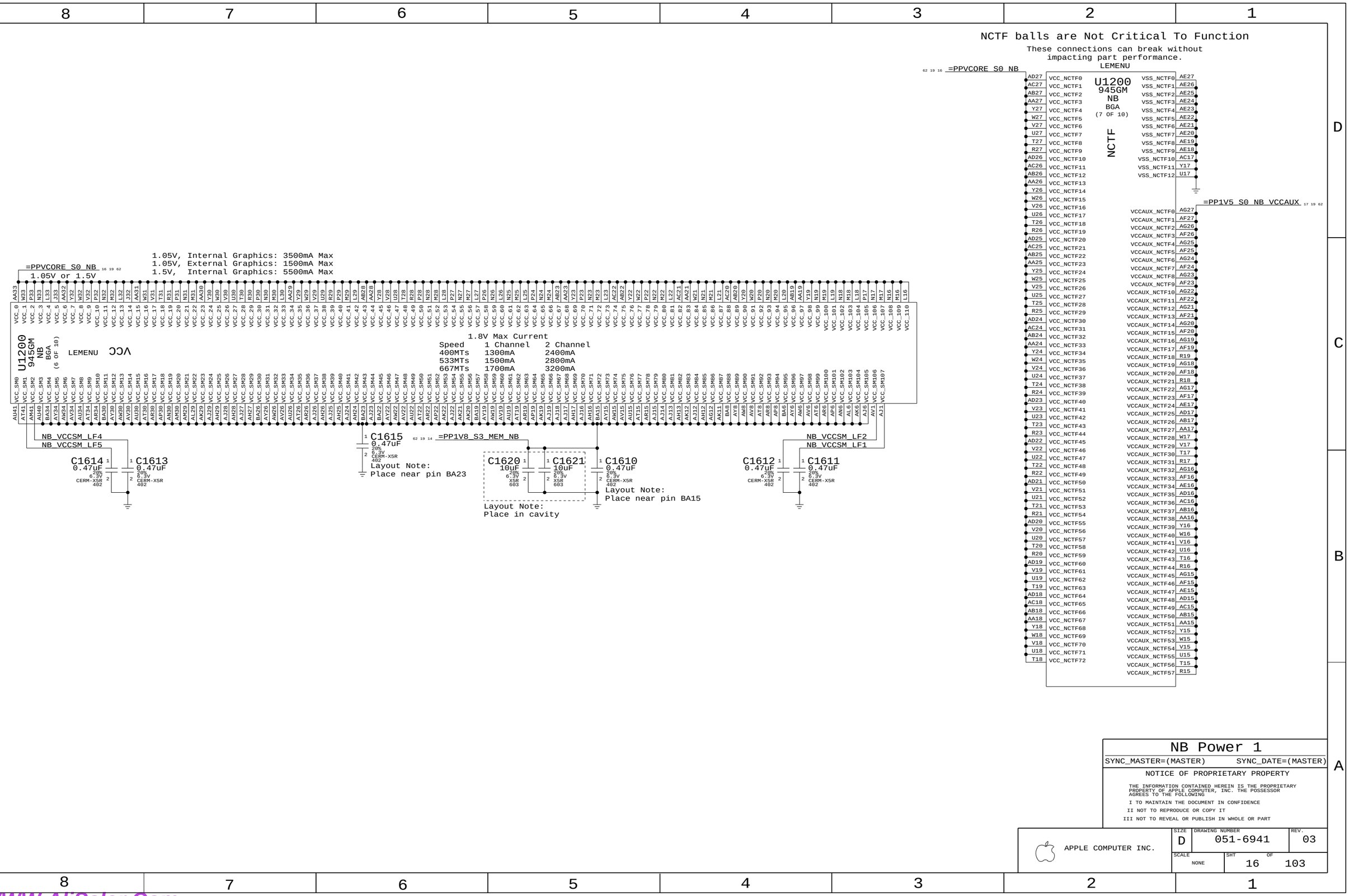

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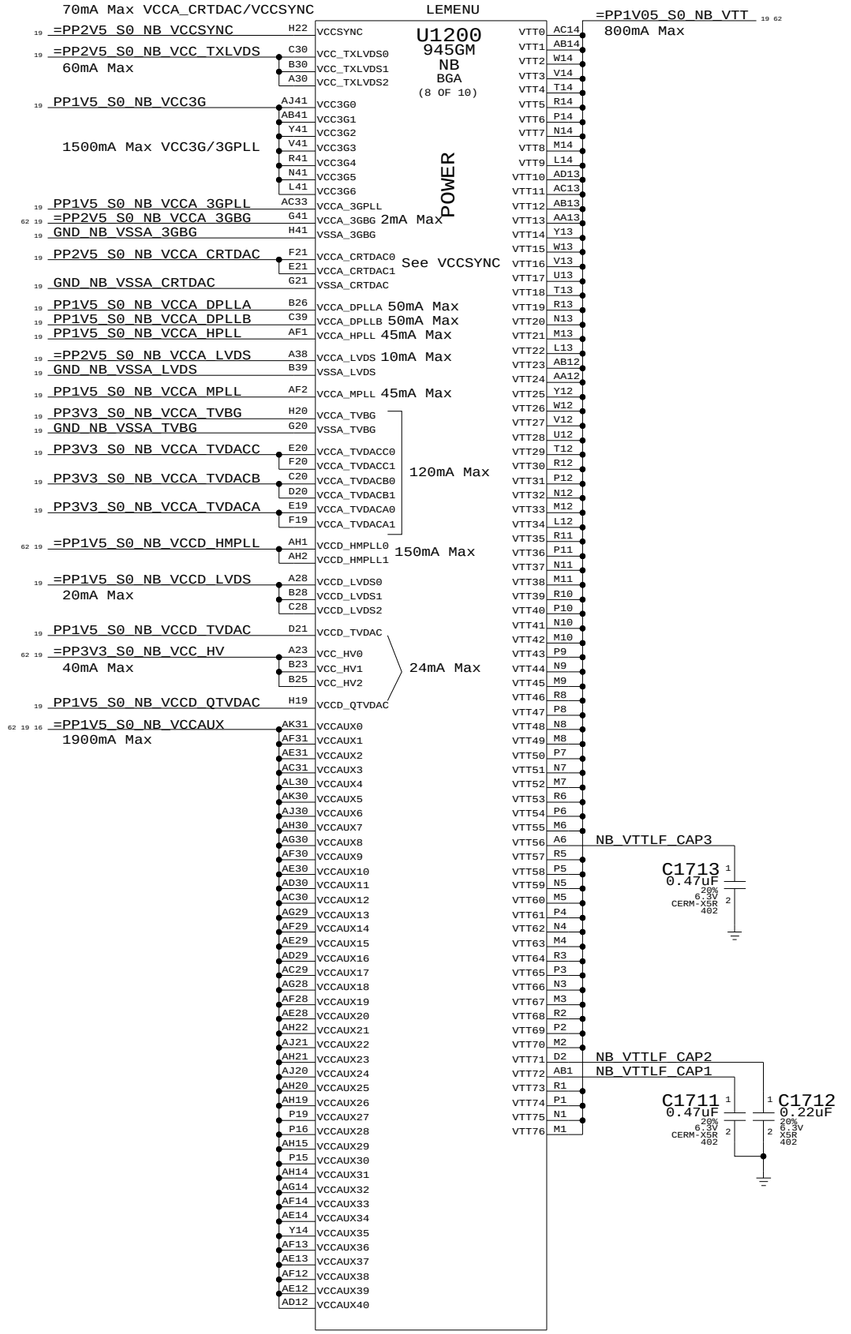

NB Power 2

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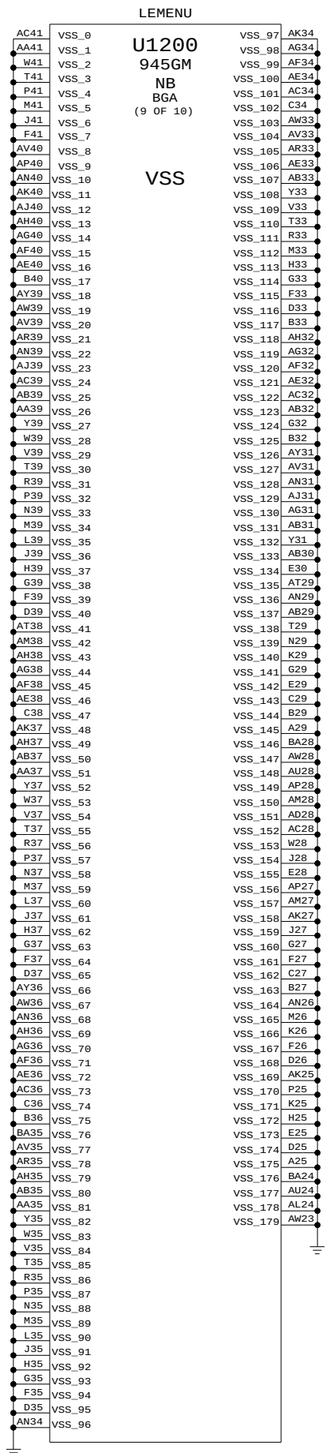

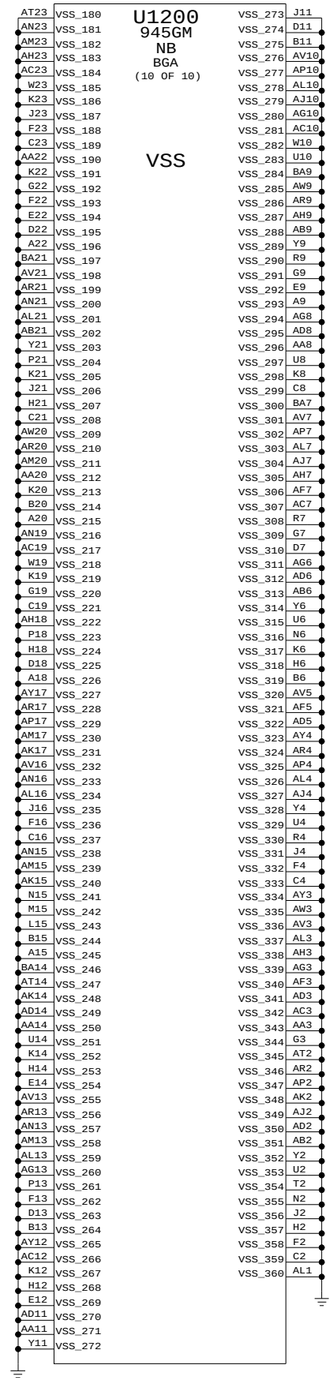

NB Grounds

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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16 19 62	1500mA Max
	=PP1V05_S0_FSB_NB	12 34 62	10mA Max?
	=PP1V05_S0_NB_VTT	17 19 62	800mA Max
	=PP1V05_S0_NB_CRT	19 62	?mA Max
3674mA Max	=PP1V5_S0_NB	62	?mA Max
	=PP1V5_S0_NB_3G	19 62	1500mA Max
	=PP1V5_S0_NB_3GPLL	19 62	
	=PP1V5_S0_NB_PCIE	13 62	?mA Max
	=PP1V5_S0_NB_PLL	19 62	100mA Max
	=PP1V5_S0_NB_TVDAC	19 62	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17 62	150mA Max
	=PP1V5_S0_NB_VCCAUX	16 17 19 62	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14 16 62	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	17 19	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	17 19	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17 19 62	2mA Max
	=PP3V3_S0_NB	14 20 62	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	17 19 62	40mA Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C1900	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

=PP1V05_S0_NB_CRT → CRT_RED, CRT_GREEN, CRT_BLUE, CRT_RED_L, CRT_GREEN_L, CRT_BLUE_L, CRT_IREF, CRT_HSYNC_R, CRT_VSYNC_R

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA

=PP1V5_S0_NB_TVDAC → TV_DACA_OUT, TV_DACB_OUT, TV_DACC_OUT, TV_IREF, TV_IRTNA, TV_IRTNB, TV_IRTNC

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL

TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA

TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB

TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK

TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA

NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG

TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN

NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH

TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL

NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P

NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N

NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0>

NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0>

NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P

NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N

NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0>

NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0>

NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34

NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35

NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27

NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28

TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK

TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS

(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS

(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS

=PPVCORE_S0_NB → (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC; GND_NB_VSSA_CRTDAC

(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC

=PP1V5_S0_NB_TVDAC → (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA; (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB; (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC; (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG; GND_NB_VSSA_TVBG

(MCH DISPLAY A PLL 1.5V PWR)

TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA

(MCH DISPLAY B PLL 1.5V PWR)

TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB

NB_CLK_DREFCLKIN_P

NB_CLK_DREFCLKIN_N

NB_CLK_DREFSSCLKIN_P

NB_CLK_DREFSSCLKIN_N

=PPVCORE_S0_NB 1500mA Max → GMCH CORE PWR 1.05V BYPASS: C1900 470UF 20% 2.5V TANT D2T; C1902 10uF 20% 6.3V X5R 603; C1903 10uF 20% 6.3V X5R 603; C1904 1uF 10% 6.3V X5R CERM 402; C1905 0.22uF 20% 6.3V X5R 402; C1906 0.22uF 20% 6.3V X5R 402; C1907 0.22uF 20% 6.3V X5R 402

=PP1V05_S0_NB_VTT 800mA Max → MCH VTT BYPASS (MCH FSB 1.05V PWR) (SHARE C0940 470UF): C1965 4.7uF 20% 6.3V CERM 603; C1966 2.2uF 20% 6.3V CERM1 603; Layout Note: Place in cavity

C1967 0.22uF 20% 6.3V X5R 402; Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV 40mA Max → MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR): C1914 10uF 20% 6.3V X5R 603; C1915 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

=PP2V5_S0_NB_VCCA_3GBG 2mA Max → C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

=PP1V5_S0_NB_VCCAUX 1900mA Max → C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_TVDAC 24mA Max → C1921 22000pF-1000mA 16V NPM18; GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB_VCCD_TVDAC; 24mA Max TVDAC/QTVDAC

C1920 0.1uF 20% 10V CERM 402

Layout Note: These 4 caps should be within 6.35 mm of NB edge

L1922 180-OHM-1.5A 0603 → PP1V5_S0_NB_QTVDAC

C1923 22000pF-1000mA 16V NPM18; GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB_VCCD_QTVDAC

C1922 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_3G 1500mA Max → L1970 91nH 2010; C1970 220UF 20% 2.5V POLY SMB2

Layout Note: Place L and C close to MCH

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR) PP1V5_S0_NB_VCC3G: C1971 10uF 20% 6.3V X5R 603; C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

1500mA Max

=PP1V5_S0_NB_3GPLL 1500mA Max → L1975 1.0UH-220MA-0.12-OHM 0805; PP1V5_S0_NB_3GPLL_F

R1975 0.51 1% 1/10W ME-LF 402

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR) PP1V5_S0_NB_VCCA_3GPLL: C1975 10uF 20% 6.3V X5R 603; C1976 0.1uF 20% 10V CERM 402; GND_NB_VSSA_3GBG

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

=PP1V5_S0_NB_PLL 100mA Max → L1934 FERR-120-OHM-0.2A 0603; GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR) PP1V5_S0_NB_VCCA_HPLL; 45mA Max

C1934 22uF 20% 6.3V X5R 805; C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603; GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR) PP1V5_S0_NB_VCCA_MPLL; 45mA Max

C1936 22uF 20% 6.3V X5R 805; C1937 0.1uF 20% 10V CERM 402

NB (GM) Decoupling

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03
SCALE: NONE	SHT: 20 OF 103	

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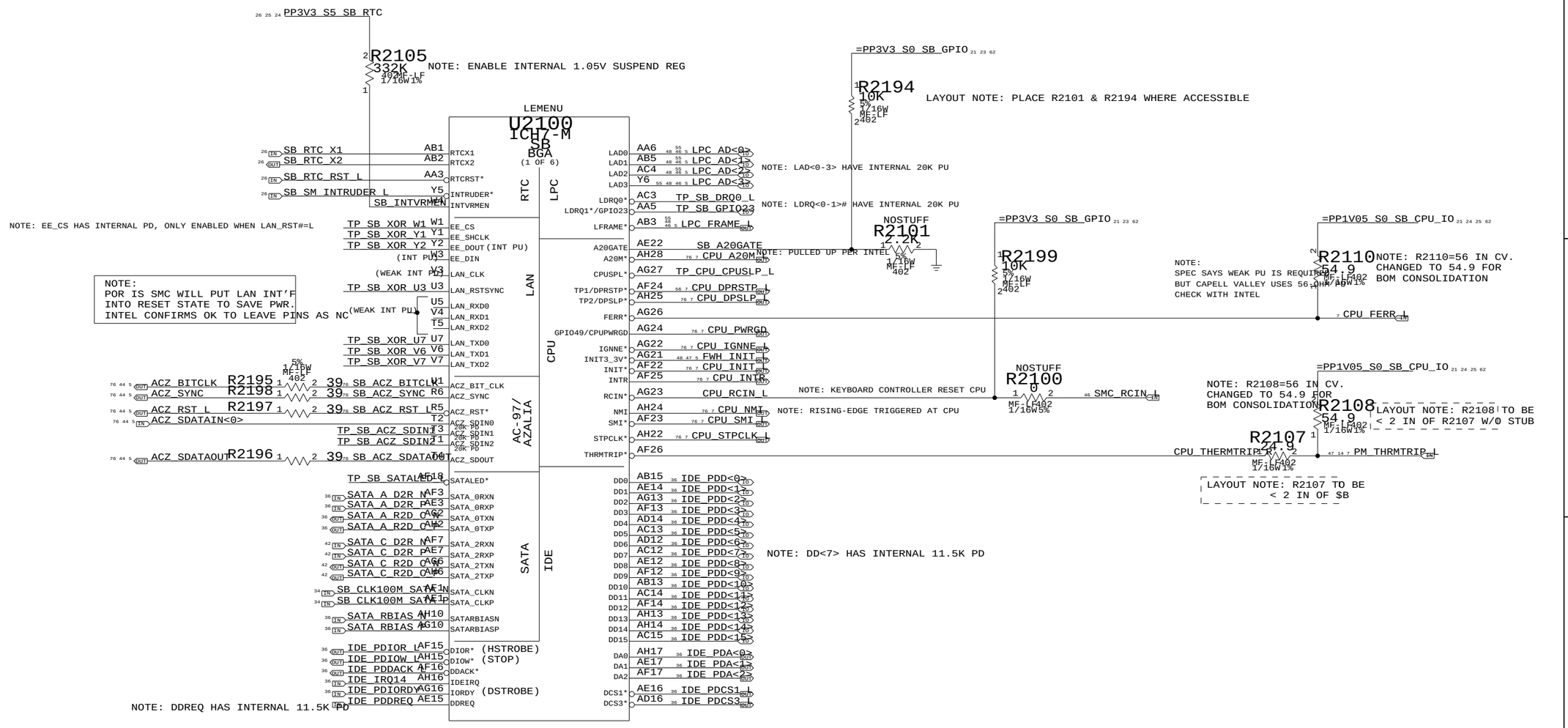

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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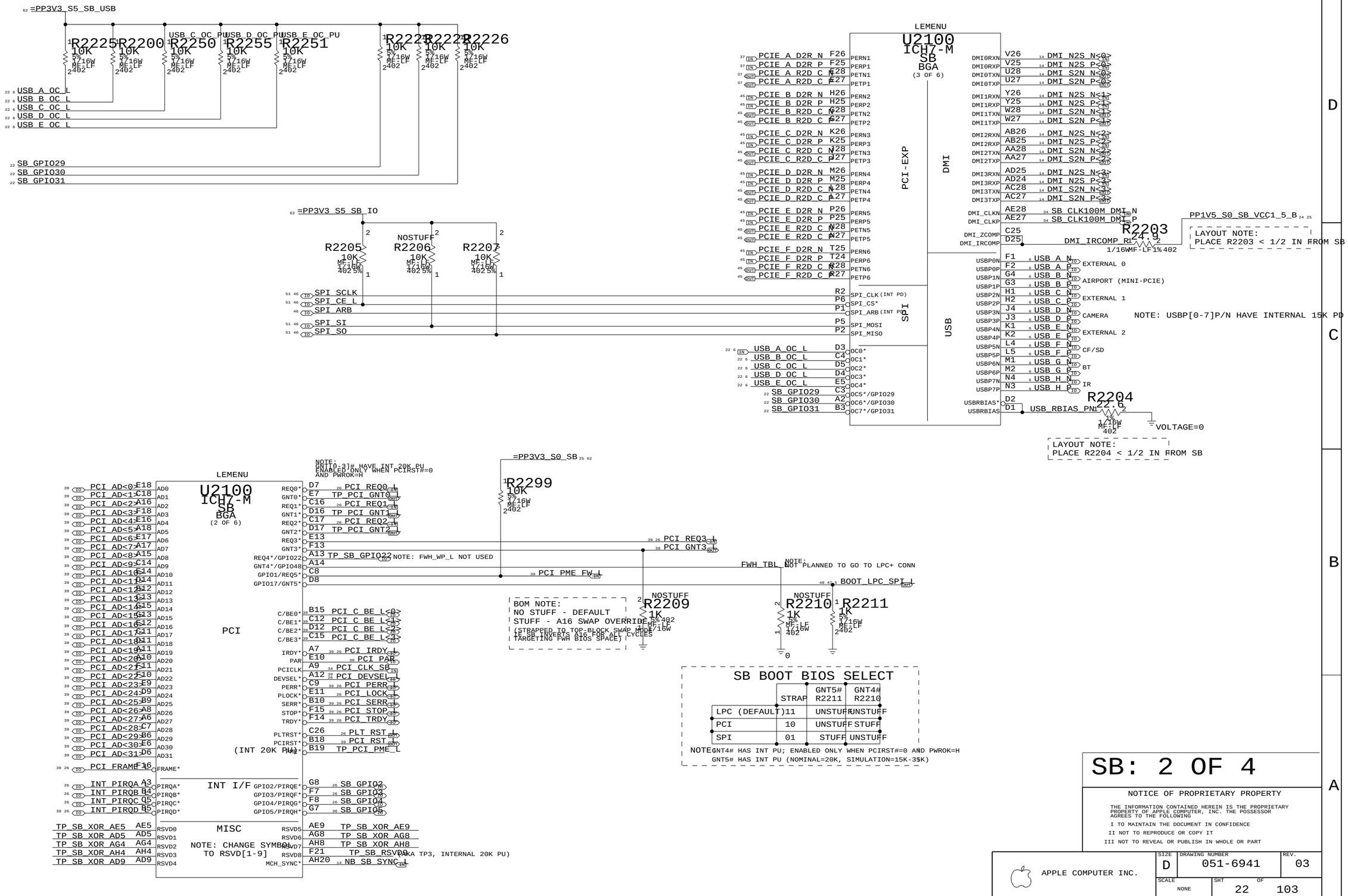

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

NO_REBOOT_MODE

RP2300 10K 5% 1/16W 8-SM-LF

R2318 10K 1/16W 2MF-LF 402 5%
R2395 8.2K 1/16W 2MF-LF 402 5%
R2396 10K 1/16W 2MF-LF 402 5%
R2397 8.2K 1/16W 2MF-LF 402 5%
R2327 NOSTUFF 10K 1/16W 2MF-LF 402 5%
R2326 NOSTUFF 10K 1/16W 2MF-LF 402 5%
R2323 1K 1/16W 2MF-LF 402 5%

=PP3V3_S5_SB 62 25 23

R2398 1K 1/16W 2MF-LF 402 5%
R2320 10K 1/16W 2MF-LF 402 5%
R2317 10K 1/16W 2MF-LF 402 5%
R2316 10K 1/16W 2MF-LF 402 5%

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U2100
ICH7-M SB
BGA
(4 OF 6)

SMB_CLK (TO) 27 — C22 SMBCLK
SMB_DATA (TO) 27 — B22 SMBDATA
SMB_LINK_ALERT_L — A16 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L (OUT) 55 48 46 5 — A27 SUS_STAT*
PM_SYSRST_L (IN) 46 26 — A22 SYS_RST*
PM_BMBUSY_L (IN) 14 — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L (OUT) 33 — AC20 GPIO18/STPPCI*
PM_STPCPU_L (OUT) 33 — AF21 GPIO20/STPCPU*
SB_GPIO26 (IN) — A21 GPIO26
BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28
PM_CLKRUN_L (TO) 55 48 46 39 5 — AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN — AC19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INTF — AZ_DOCK_RST — U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L (IN) 44 37 5 — F20 WAKE*
INT_SERIRQ (TO) 55 48 46 5 — AH21 SERIRQ
PM_THRM_L (IN) 46 — AF20 THRM*
VR_PWRGD_CK410 (IN) 26 — AD22 VRMPWRGD
TP_SB_GPIO6 (TO) — AG21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
SB_EXTSMI_L — E21 GPIO8

SMB

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
SATA_C_DET_L (IN) 36

CLKS

CLK14 — AC1 — 34 SB_CLK14P3M_TIMER (IN)
CLK48 — B2 — 34 SB_CLK48M_USBCTLR (IN)
SUSCLK — C20 — 8 SUS_CLK_SB (OUT)

SYS GPIO / PWR MNGT

SLP_S3* — B24 — 64 46 PM_SLP_S3_L (OUT)
SLP_S4* — D23 — 64 46 PM_SLP_S4_L (OUT)
SLP_S5* — F22 — 46 PM_SLP_S5_L (OUT)
PWROK — AA4 — 26 PM_SB_PWROK (IN)
GPIO16/DPRSLPVR — AC22 — 76 56 14 PM_DPRSLPVR (OUT)
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
TP0/BATLOW* — C21 — PM_BATLOW_L (IN) 46
PWRBTN* — C23 — 46 PM_PWRBTN_L (IN)
(INT 20K PU)
LAN_RST* — C19 — 46 PM_LAN_ENABLE (IN)
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4 — PM_RSMRST_L (IN) 46

GPIO

GPIO9 — E20 — 47 46 SMS_INT_L (IN)
GPIO10 — A20 — 46 SMC_SB_NMI (IN)
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L (OUT)
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 36 23 IDE_RESET_L (OUT)
GPIO15 — E22 — SV_SET_UP 5 23 48
GPIO24 — R3 — CRB_SV_DET 23
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L (OUT)
GPIO38 — AD20 — TP_SB_GPIO38 (NC)
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L (OUT)

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 2MF-LF 402 5%
R2343 8.2K 1/16W 2MF-LF 402 5%

R2399 100K 1/16W 2MF-LF 402 5%

NOSTUFF
R2300 0 1/16W 2MF-LF 402 5%
SMC_RUNTIME_SCI_L (IN) 46
SMC_EXTSMI_L (IN) 46
R2301 0 1/16W 2MF-LF 402 5%

=PP3V3_S0_SB_GPIO 62 23 21

R2306 NOSTUFF 10K 1/16W 2MF-LF 402 5%
R2308 10K 1/16W 2MF-LF 402 5%
SV_SET_UP 5 23 48
CRB_SV_DET 23
R2307 10K 1/16W 2MF-LF 402 5%
R2309 NOSTUFF 0 1/16W 2MF-LF 402 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

=PP3V3_S5_SB 62 25 23

R2313 10K 1/16W 2MF-LF 402 5%
R2310 10K 1/16W 2MF-LF 402 5%
FWH_MFG_MODE 23
BIOS_REC 23
R2314 NOSTUFF 0 1/16W 2MF-LF 402 5%
R2311 NOSTUFF 10K 1/16W 2MF-LF 402 5%

=PP3V3_S0_SB_GPIO 21 23 62

R2390 10K 1/16W 2MF-LF 402 5%
R2389 10K 1/16W 2MF-LF 402 5%
R2388 10K 1/16W 2MF-LF 402 5%
PATA_PWR_EN_L 23
IDE_RESET_L 36 23
SATA_C_PWR_EN_L 23

SB: 3 OF 4

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(6 OF 6)

VSS

A4 A23 N24 P24 R18 U14 V27 AA24 AB27 AD11 B1 D10 F4 G18 J1 L24 M17 N14 N17 N18 N25 N26 P3 P4 P12 P13 P14 P15 P16 P17 P27 P28 R1 R11 R12 R13 R14 R15 R16 R17 T6 T12 T13 T14 T15 T16 T17 U4 U12 U13 U15 U16 U17 U24 U25 U26 V2 V13 V15 V24 V28 W6 W24 W25 W26 Y3 Y24 Y27 Y28 AA1 AA25 AA26 AB4 AB6 AB11 AB14 AB16 AB19 AB21 AB24 AB28 AC2 AC5 AC9 AC11 AD1 AE24 AE25 AF2 AF4 AF8 AF11 AF27 AF28 AG1 AG3 AG7

AD3 AD4 AD7 AD8 AD15 AD19 AD23 AE2 AE4 AE8 AE11 AE13 AE18 AE21 B8 B11 B14 B17 B20 B26 B28 C2 C6 C27 D13 D18 D21 D24 E1 E2 E4 E8 E15 F3 F5 F12 F27 F28 G1 G2 G5 G6 G9 G14 G21 G24 G25 G26 H3 H4 H5 H24 H27 H28 J2 J5 J24 J25 J26 K24 K27 K28 L13 L15 L25 L26 M3 M4 M5 M12 M13 M14 M15 M16 M24 M27 M28 N1 N2 N5 N6 N11 N12 N13 N15 N16 AG11 AG14 AG17 AG20 AG25 AH1 AH3 AH7 AH12 AH23 AH27

0 0

LEMENU

U2100
ICH7-M
SB
BGA
(5 OF 6)

25 PP5V_S0_SB_V5REF
25 PP5V_S5_SB_V5REF_SUS
25 22 PP1V5_S0_SB_VCC1_5_A

G10 AD17 V5REF
F9 V5REF_SUS
AA22 AA23 AB22 AB23 AC23 AC24 AC25 AC26 AD26 AD27 AD28 D26 D27 D28 E24 E25 E26 F23 F24 G22 G23 H22 H23 J22 J23 K22 K23 L22 L23 M22 M23 N22 N23 P22 P23 R22 R23 R24 R25 R26 T22 T23 T26 T27 T28 U22 U23 V22 V23 W22 W23 Y22 Y23

VCCA3GP
VCC1_5_B

62 25 24 =PP3V3_S0_SB_VCC3_3
25 PP1V5_S0_SB_VCCDMIPLL
62 25 =PP1V5_S0_SB_VCC1_5_A_ARX
62 25 =PP1V5_S0_SB_VCCSATAPLL
62 25 24 =PP3V3_S0_SB_VCC3_3
62 25 =PP1V5_S0_SB_VCC1_5_A_ATX
62 25 24 =PP3V3_S5_SB_VCCSUS3_3
62 25 =PP1V5_S0_SB_VCCUSBPLL

E27 VCC3_3
AG28 VCCDMIPLL
AB7 AC6 AC7 AD6 AE6 AF5 AF6 AG5 AH5 ARX
VCC1_5_A
AD2 VCCSATAPLL
AH11 VCC3_3
AB10 AB9 AC10 AD10 AE10 AF10 AF9 AG9 AH9 ATX
VCC1_5_A
F3 VCCSUS3_3
C1 VCCUSBPLL
A2 VCCLAN1_5
Y7 CHANGE SYMBOL TO 1.0V

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

CORE
VCC1_05

L11 L12 L14 L16 L17 L18 M11 M18 P11 P18 T11 T18 U11 U18 V11 V12 V14 V16 V17 V18

=PPVCORE_S0_SB 25 62

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

VCC_PAUX
VCCLAN_3_3

V5 V1 W2 W7

=PP3V3_S0_SB_VCCLAN3_3 25 62

VCC3_3/VCCHDA
VCCSUS3_3/VCCSUSHDA

U6 =PP3V3_S0_SB_3V3_1V5_VCCHDA
R7 =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

AE23 =PP1V05_S0_SB_CPU_IO 21 25 62
V_CPU_IO
AE26 AH26

IDE
VCC3_3

AA7 AB12 AB20 AC16 AD13 AD18 AG12 AG15 AG19

=PP3V3_S0_SB_VCC3_3_IDE 25 62

PCI
VCC3_3

A5 B13 B16 B7 C10 D15 F9 G11 G12 G16

=PP3V3_S0_SB_VCC3_3_PCI 25 62

VCCRTC
W5 PP3V3_S5_SB_RTC 21 25 26

P7 =PP3V3_S5_SB_VCCSUS3_3 24 25 62

USB
VCCSUS3_3

A24 C24 D19 D22 G19 K3 K4 K5 K6 L1 L2 L3 L6 L7 M6 M7 N7

=PP3V3_S5_SB_VCCSUS3_3_USB 25 62

VCC1_5_A
AB17 AC17 T7 F17 G17 AB8 AC8

=PP1V5_S0_SB_VCC1_5_A 25 62

VCCSAUS1_5
CHANGE SYMBOL TO 1.0V

K7 C28 G20

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

USB CORE
VCC1_5_A

A1 H6 H7 J6 J7

=PP1V5_S0_SB_VCC1_5_A_USB_CORE

SB: 4 OF 4

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NONE	24	103

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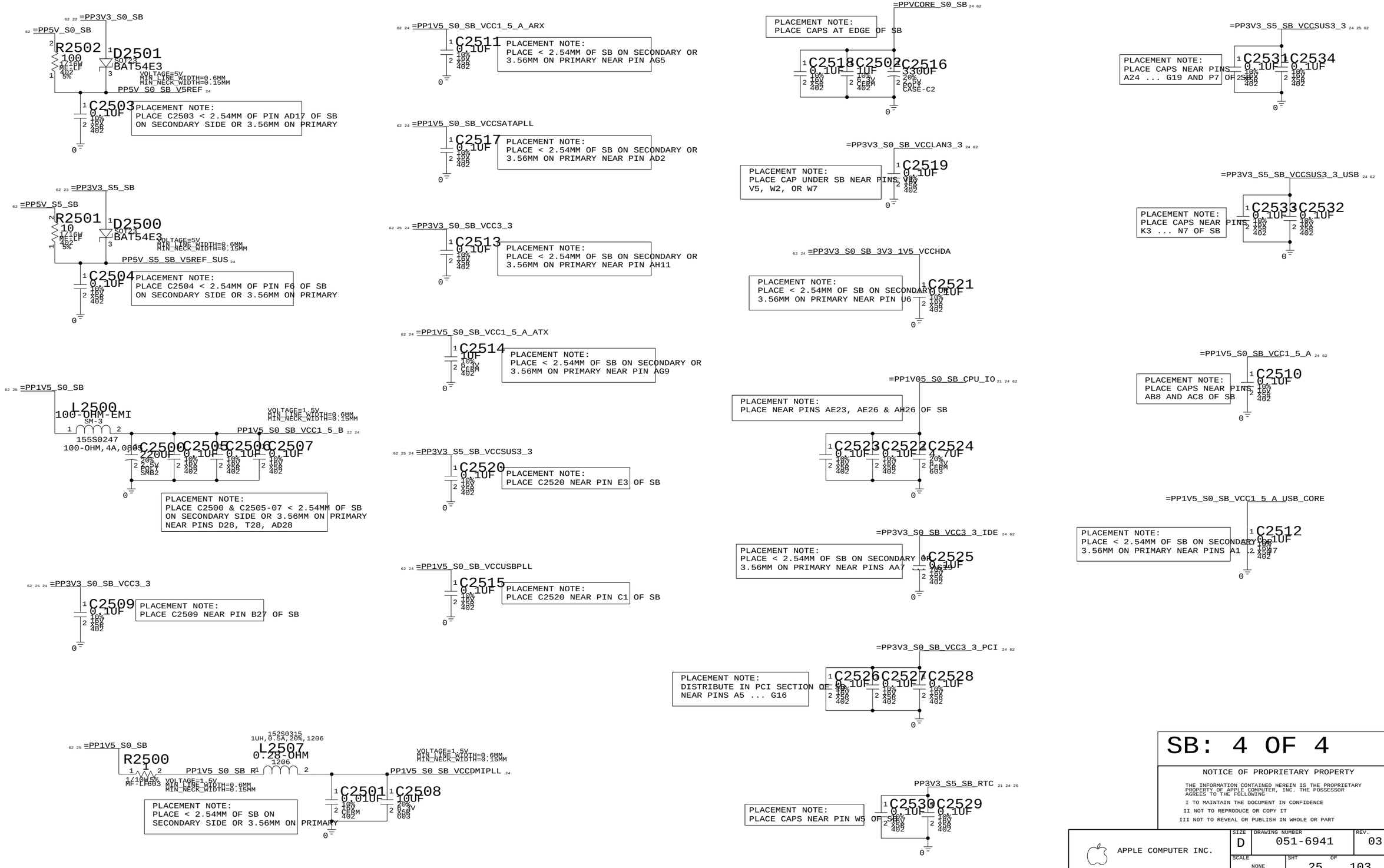

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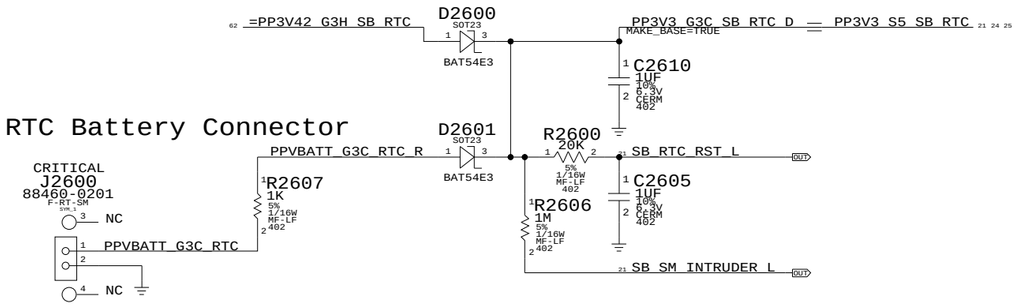
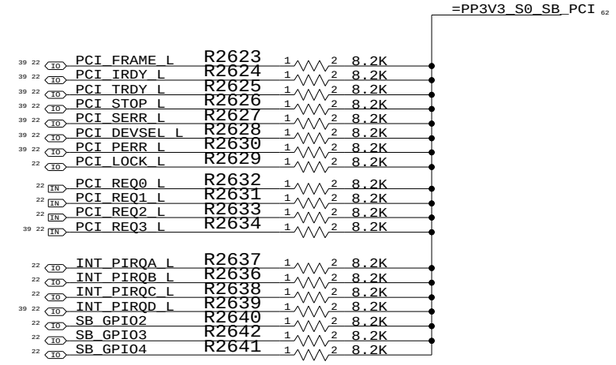
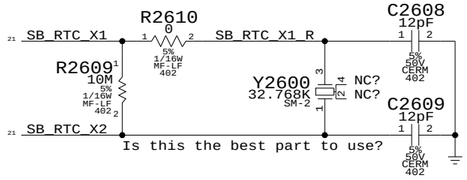
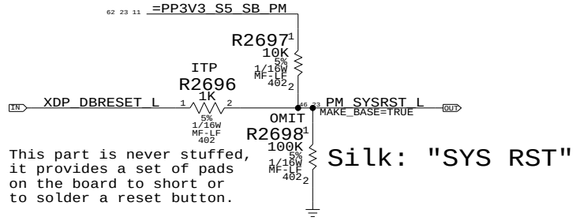
RTC Battery Connector





SB RTC Crystal Circuit

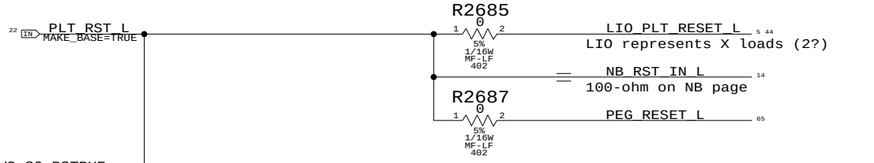




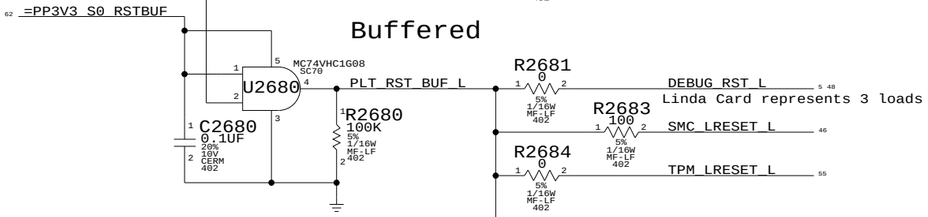
This part is never stuffed,
it provides a set of pads
on the board to short or
to solder a reset button.

Platform Reset Connections

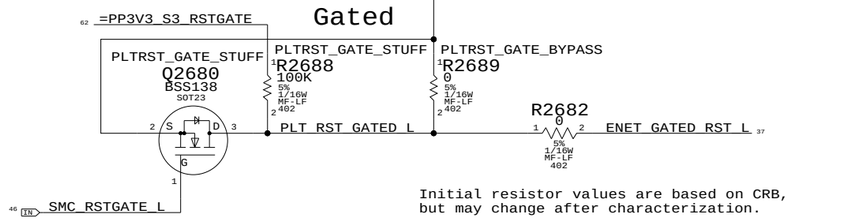
Unbuffered



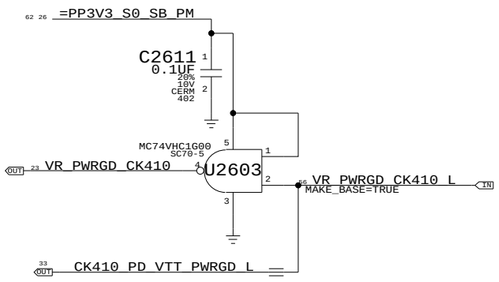
Buffered



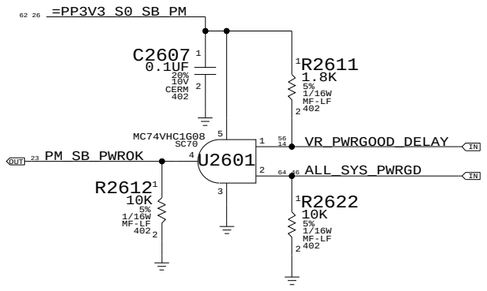
Gated



Initial resistor values are based on CRB,
but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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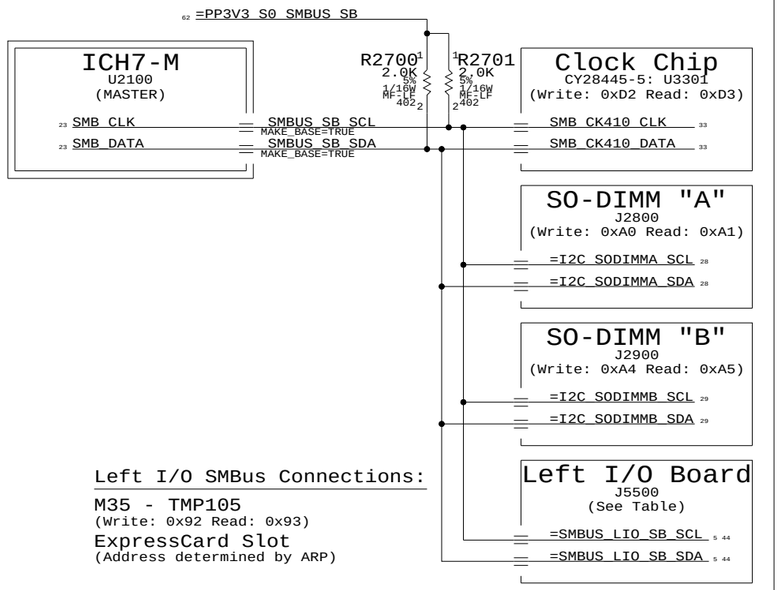
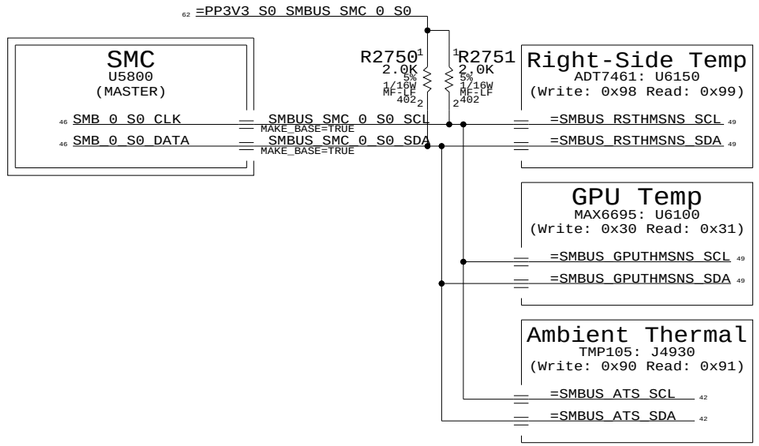
ICH7-M SMBus Connections

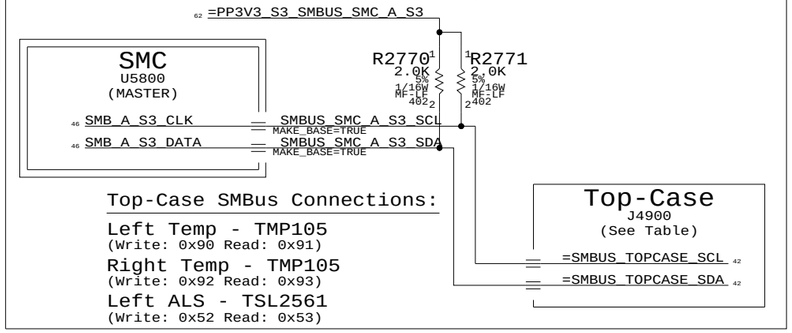


SMC "0" SMBus Connections

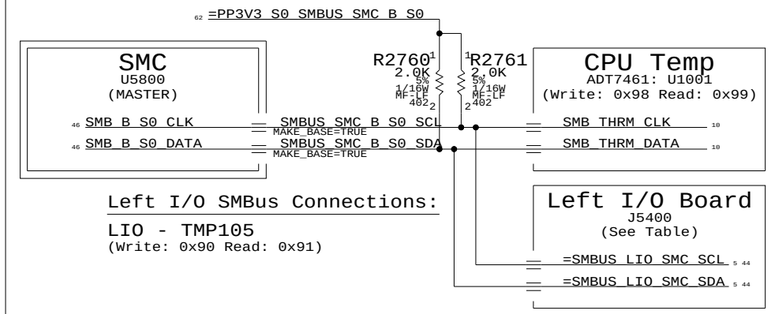


SMC "A" SMBus Connections

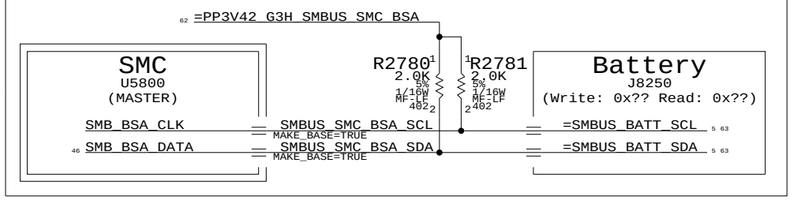
NOTE: SMC RMT bus remains powered and may be active in S3 state



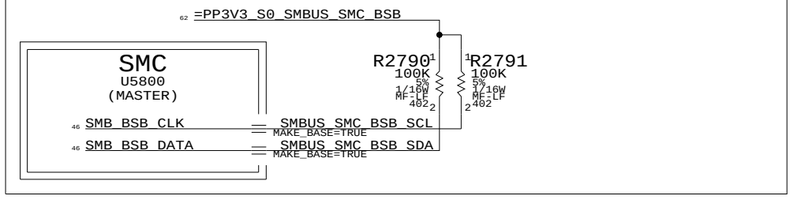
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	27	103

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Page Notes

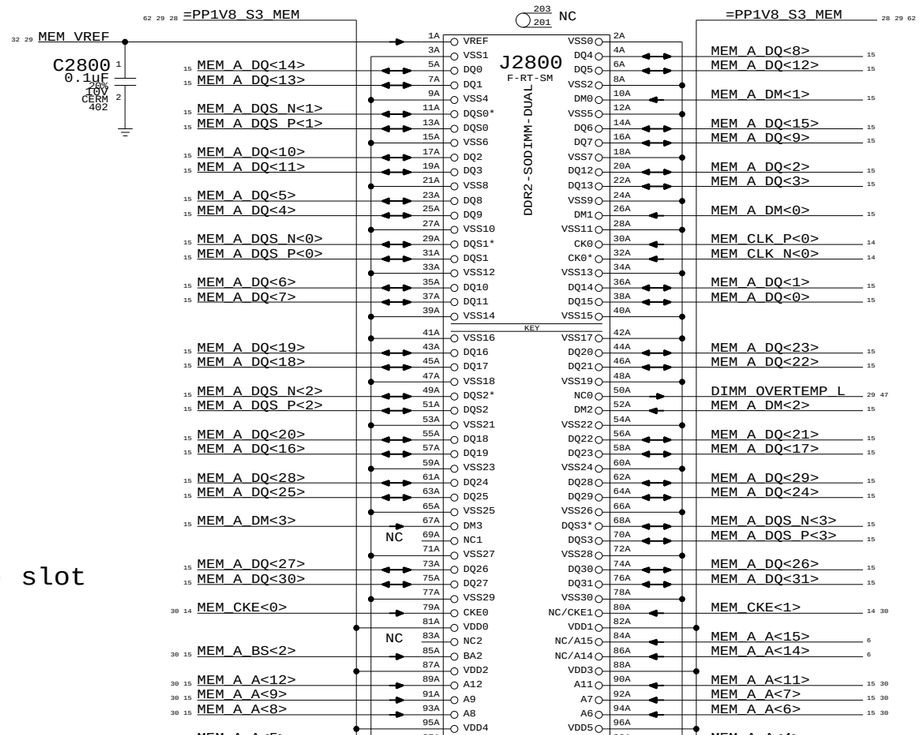
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

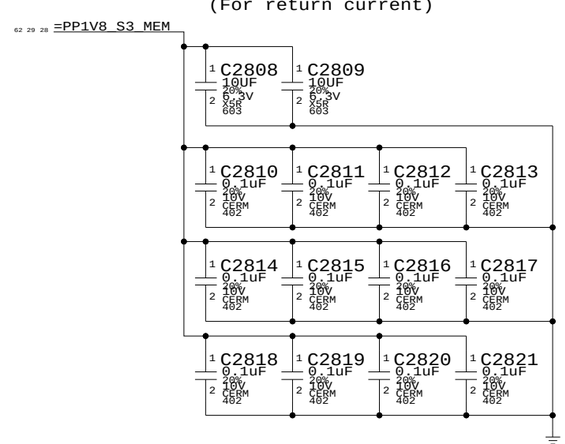
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot





DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 28 OF 103	

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot

62 29 28 =PP1V8_S3_MEM

32 28 MEM_VREF

C2900 0.1uF 20% 10V CERM 402

J2900 F-RT-TH DDR2-SODIMM-DUAL

		1B	VREF	VSS0	2B		
		3B	VSS1	DQ4	4B	MEM_B_DQ<9>	15
15	MEM_B_DQ<15>	5B	DQ0	DQ5	6B	MEM_B_DQ<11>	15
15	MEM_B_DQ<14>	7B	DQ1	VSS2	8B		
		9B	VSS4	DM0	10B	MEM_B_DM<1>	15
15	MEM_B_DQS_N<1>	11B	DQS0*	VSS5	12B		
15	MEM_B_DQS_P<1>	13B	DQS0	DQ6	14B	MEM_B_DQ<12>	15
		15B	VSS6	DQ7	16B	MEM_B_DQ<8>	15
15	MEM_B_DQ<10>	17B	DQ2	VSS7	18B		
15	MEM_B_DQ<13>	19B	DQ3	DQ12	20B	MEM_B_DQ<3>	15
		21B	VSS8	DQ13	22B	MEM_B_DQ<6>	15
15	MEM_B_DQ<7>	23B	DQ8	VSS9	24B		
15	MEM_B_DQ<2>	25B	DQ9	DM1	26B	MEM_B_DM<0>	15
		27B	VSS10	VSS11	28B		
15	MEM_B_DQS_N<0>	29B	DQS1*	CK0	30B	MEM_CLK_P<3>	14
15	MEM_B_DQS_P<0>	31B	DQS1	CK0*	32B	MEM_CLK_N<3>	14
		33B	VSS12	VSS13	34B		
15	MEM_B_DQ<1>	35B	DQ10	DQ14	36B	MEM_B_DQ<0>	15
15	MEM_B_DQ<4>	37B	DQ11	DQ15	38B	MEM_B_DQ<5>	15
		39B	VSS14	VSS15	40B		
			KEY				
		41B	VSS16	VSS17	42B		
15	MEM_B_DQ<21>	43B	DQ16	DQ20	44B	MEM_B_DQ<22>	15
15	MEM_B_DQ<19>	45B	DQ17	DQ21	46B	MEM_B_DQ<18>	15
		47B	VSS18	VSS19	48B		
15	MEM_B_DQS_N<2>	49B	DQS2*	NC0	50B	DIMM_OVERTEMP_L	28 47
15	MEM_B_DQS_P<2>	51B	DQS2	DM2	52B	MEM_B_DM<2>	15
		53B	VSS21	VSS22	54B		
15	MEM_B_DQ<20>	55B	DQ18	DQ22	56B	MEM_B_DQ<17>	15
15	MEM_B_DQ<23>	57B	DQ19	DQ23	58B	MEM_B_DQ<16>	15
		59B	VSS23	VSS24	60B		
15	MEM_B_DQ<29>	61B	DQ24	DQ28	62B	MEM_B_DQ<26>	15
15	MEM_B_DQ<24>	63B	DQ25	DQ29	64B	MEM_B_DQ<28>	15
		65B	VSS25	VSS26	66B		
15	MEM_B_DM<3>	67B	DM3	DQS3*	68B	MEM_B_DQS_N<3>	15
	NC	69B	NC1	DQS3	70B	MEM_B_DQS_P<3>	15
		71B	VSS27	VSS28	72B		
15	MEM_B_DQ<27>	73B	DQ26	DQ30	74B	MEM_B_DQ<31>	15
15	MEM_B_DQ<25>	75B	DQ27	DQ31	76B	MEM_B_DQ<30>	15
		77B	VSS29	VSS30	78B		
30 14	MEM_CKE<2>	79B	CKE0	NC/CKE1	80B	MEM_CKE<3>	14 30
		81B	VDD0	VDD1	82B		
	NC	83B	NC2	NC/A15	84B	MEM_B_A<15>	6
30 15	MEM_B_BS<2>	85B	BA2	NC/A14	86B	MEM_B_A<14>	6
		87B	VDD2	VDD3	88B		
30 15	MEM_B_A<12>	89B	A12	A11	90B	MEM_B_A<11>	15 30
30 15	MEM_B_A<9>	91B	A9	A7	92B	MEM_B_A<7>	15 30
30 15	MEM_B_A<8>	93B	A8	A6	94B	MEM_B_A<6>	15 30
		95B	VDD4	VDD5	96B		
30 15	MEM_B_A<5>	97B	A5	A4	98B	MEM_B_A<4>	15 30
30 15	MEM_B_A<3>	99B	A3	A2	100B	MEM_B_A<2>	15 30
30 15	MEM_B_A<1>	101B	A1	A0	102B	MEM_B_A<0>	15 30
		103B	VDD6	VDD7	104B		
30 15	MEM_B_A<10>	105B	A10/AP	BA1	106B	MEM_B_BS<1>	15 30
30 15	MEM_B_BS<0>	107B	BA0	RAS*	108B	MEM_B_RAS_L	15 30
30 15	MEM_B_WE_L	109B	WE*	S0*	110B	MEM_CS_L<2>	14 30
		111B	VDD8	VDD9	112B		
30 15	MEM_B_CAS_L	113B	CAS*	ODT0	114B	MEM_ODT<2>	14 30
30 14	MEM_CS_L<3>	115B	NC/S1*	NC/A13	116B	MEM_B_A<13>	15 30
		117B	VDD10	VDD11	118B		
30 14	MEM_ODT<3>	119B	NC/ODT1	NC3	120B	NC	
		121B	VSS31	VSS32	122B		
15	MEM_B_DQ<36>	123B	DQ32	DQ36	124B	MEM_B_DQ<32>	15
15	MEM_B_DQ<33>	125B	DQ33	DQ37	126B	MEM_B_DQ<37>	15
		127B	VSS33	VSS34	128B		
15	MEM_B_DQS_N<4>	129B	DQS4*	DM4	130B	MEM_B_DM<4>	15
15	MEM_B_DQS_P<4>	131B	DQS4	VSS35	132B		
		133B	VSS36	DQ38	134B	MEM_B_DQ<38>	15
15	MEM_B_DQ<34>	135B	DQ34	DQ39	136B	MEM_B_DQ<39>	15
15	MEM_B_DQ<35>	137B	DQ35	VSS37	138B		
		139B	VSS38	DQ44	140B	MEM_B_DQ<44>	15
15	MEM_B_DQ<40>	141B	DQ40	DQ45	142B	MEM_B_DQ<45>	15
15	MEM_B_DQ<41>	143B	DQ41	VSS39	144B		
		145B	VSS40	DQS5*	146B	MEM_B_DQS_N<5>	15
15	MEM_B_DM<5>	147B	DM5	DQS5	148B	MEM_B_DQS_P<5>	15
		149B	VSS41	VSS42	150B		
15	MEM_B_DQ<42>	151B	DQ42	DQ46	152B	MEM_B_DQ<46>	15
15	MEM_B_DQ<43>	153B	DQ43	DQ47	154B	MEM_B_DQ<47>	15
		155B	VSS43	VSS44	156B		
15	MEM_B_DQ<62>	157B	DQ48	DQ52	158B	MEM_B_DQ<58>	15
15	MEM_B_DQ<59>	159B	DQ49	DQ53	160B	MEM_B_DQ<63>	15
		161B	VSS45	VSS46	162B		
	NC	163B	NC_TEST	CK1	164B	MEM_CLK_P<2>	14
		165B	VSS47	CK1*	166B	MEM_CLK_N<2>	14
15	MEM_B_DQS_N<7>	167B	DQS6*	VSS48	168B		
15	MEM_B_DQS_P<7>	169B	DQS6	DM6	170B	MEM_B_DM<7>	15
		171B	VSS49	VSS50	172B		
15	MEM_B_DQ<60>	173B	DQ50	DQ54	174B	MEM_B_DQ<56>	15
15	MEM_B_DQ<61>	175B	DQ51	DQ55	176B	MEM_B_DQ<57>	15
		177B	VSS51	VSS52	178B		
15	MEM_B_DQ<54>	179B	DQ56	DQ60	180B	MEM_B_DQ<55>	15
15	MEM_B_DQ<51>	181B	DQ57	DQ61	182B	MEM_B_DQ<50>	15
		183B	VSS53	VSS54	184B		
15	MEM_B_DM<6>	185B	DM7	DQS7*	186B	MEM_B_DQS_N<6>	15
		187B	VSS55	DQS7	188B	MEM_B_DQS_P<6>	15
15	MEM_B_DQ<52>	189B	DQ58	VSS56	190B		
15	MEM_B_DQ<49>	191B	DQ59	DQ62	192B	MEM_B_DQ<53>	15
62 29 28	=PPSPD_S0_MEM	193B	VSS57	DQ63	194B	MEM_B_DQ<48>	15
27	=I2C_SODIMMB_SDA	195B	SDA	VSS58	196B		
27	=I2C_SODIMMB_SCL	197B	SCL	SA0	198B		
		199B	VDDSPD	SA1	200B		

516-0130

20 NC

202 NC

=PP1V8_S3_MEM 28 29 62

=PPSPD_S0_MEM 28 29 62

R2900 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

SODIMM_A_SA1

ADDR=0xA4(WR)/0xA5(RD)

DDR2 Bypass Caps

(For return current)

62 29 28 =PP1V8_S3_MEM

C2908	10UF 20% 6.3V X5R 603	C2909	10UF 20% 6.3V X5R 603
C2910	0.1uF 20% 10V CERM 402	C2911	0.1uF 20% 10V CERM 402
C2912	0.1uF 20% 10V CERM 402	C2913	0.1uF 20% 10V CERM 402
C2914	0.1uF 20% 10V CERM 402	C2915	0.1uF 20% 10V CERM 402
C2916	0.1uF 20% 10V CERM 402	C2917	0.1uF 20% 10V CERM 402
C2918	0.1uF 20% 10V CERM 402	C2919	0.1uF 20% 10V CERM 402
C2920	0.1uF 20% 10V CERM 402	C2921	0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03
SCALE: NONE	SHT 29 OF 103	

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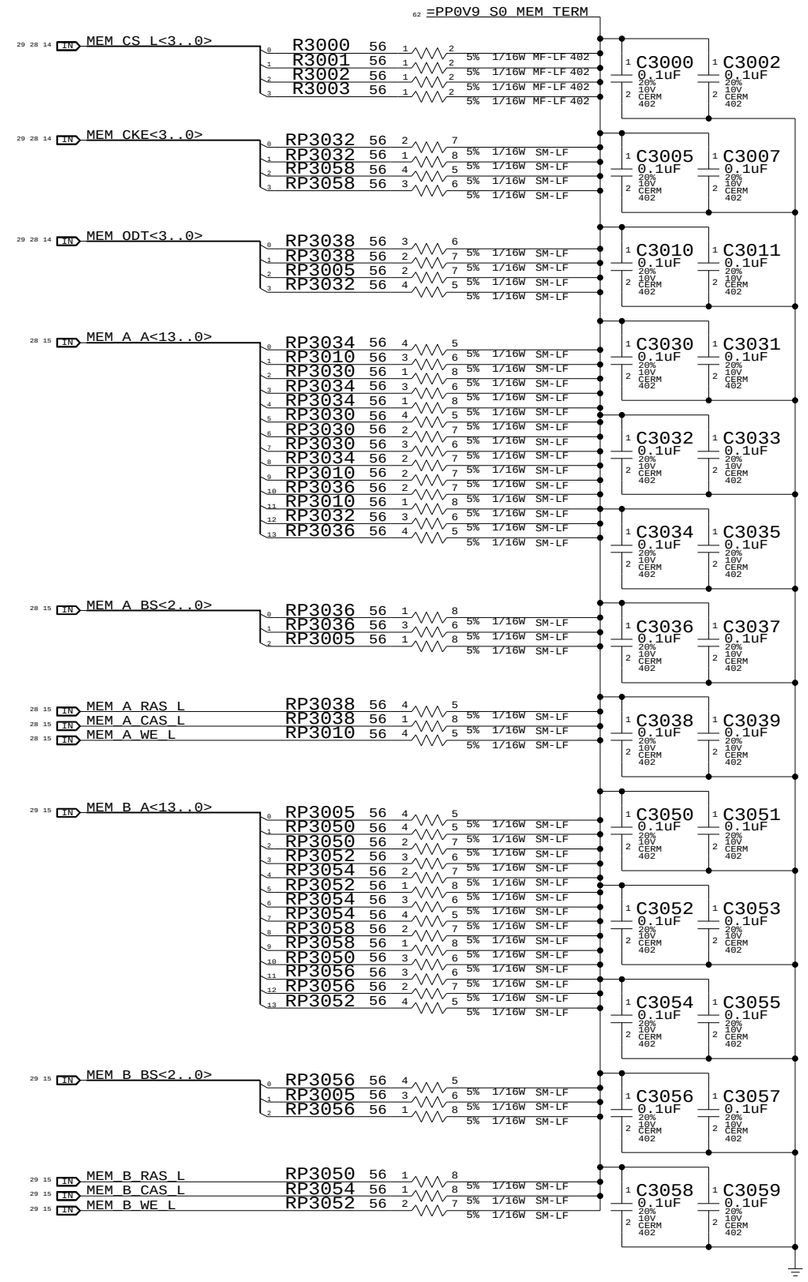
One cap for each side of every RPAK, one cap for every two discrete resistors



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

SCALE	SHT	OF
NONE	30	103

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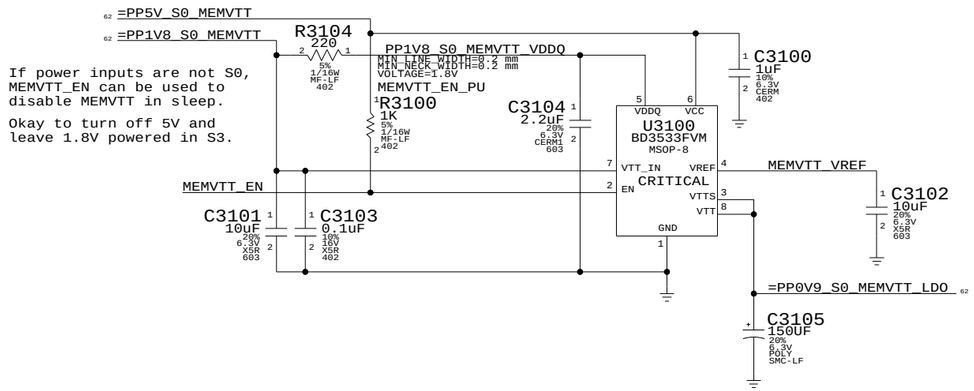
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

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SCALE	SHT	OF
NONE	31	103

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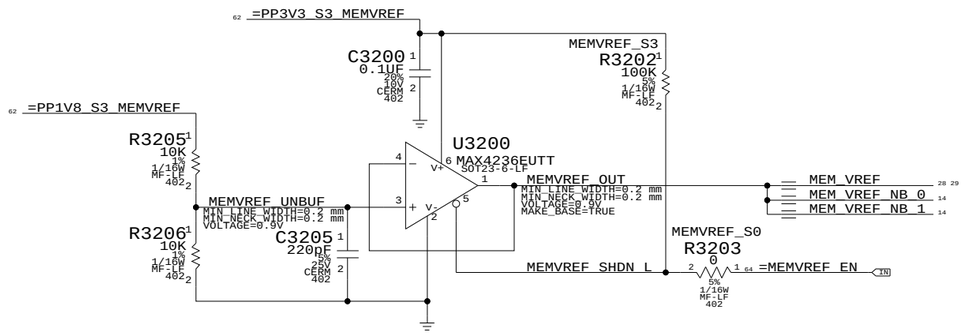

DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

SCALE	SHT	OF
NONE	32	103

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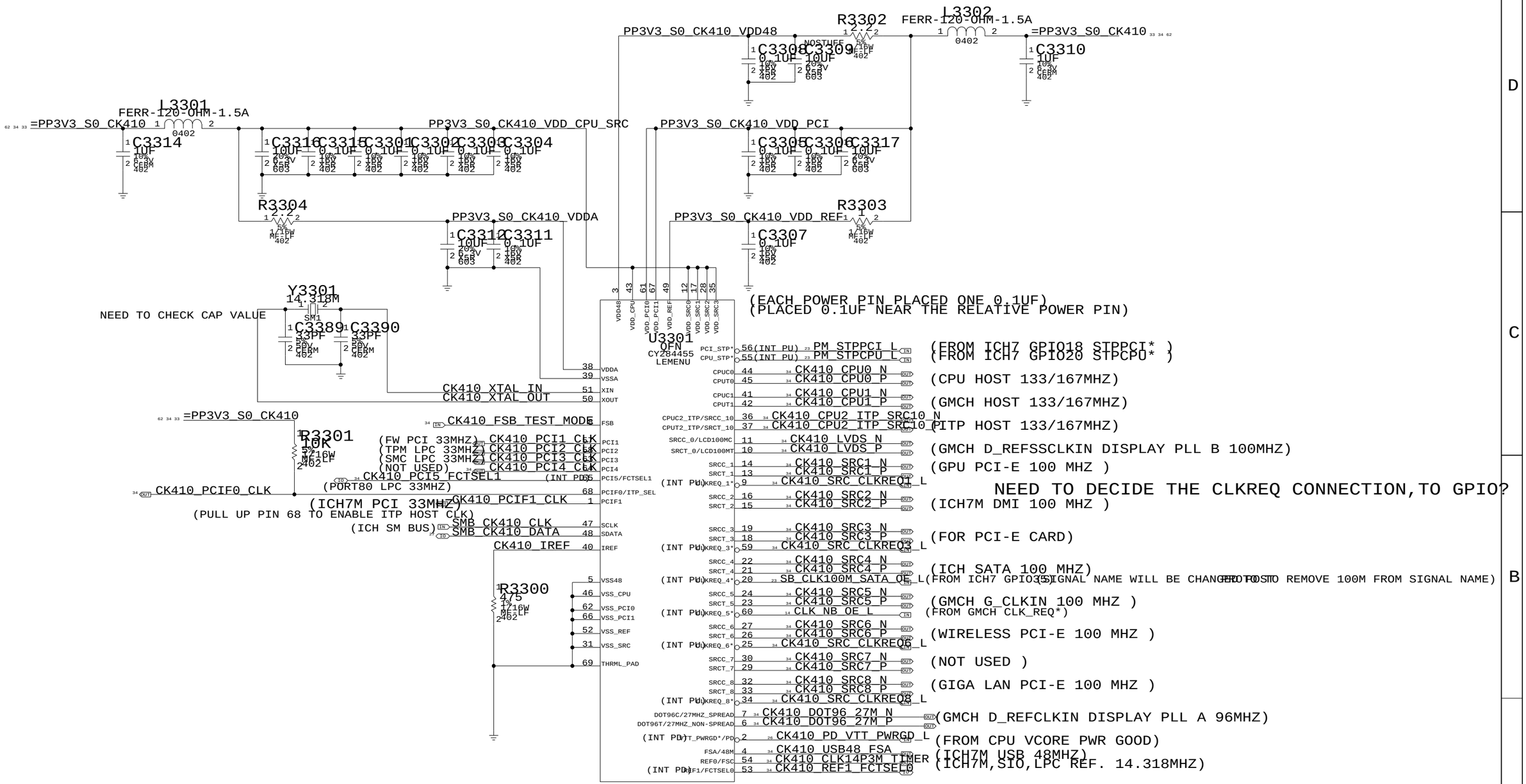

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON-SPREAD	27M_SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

CLOCKS

SYNC_MASTER=MBZ SYNC_DATE=08/04/2005

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D	051-6941	03

SCALE	SHT	OF
NONE	33	103

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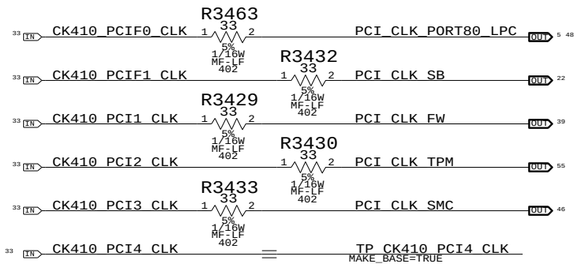
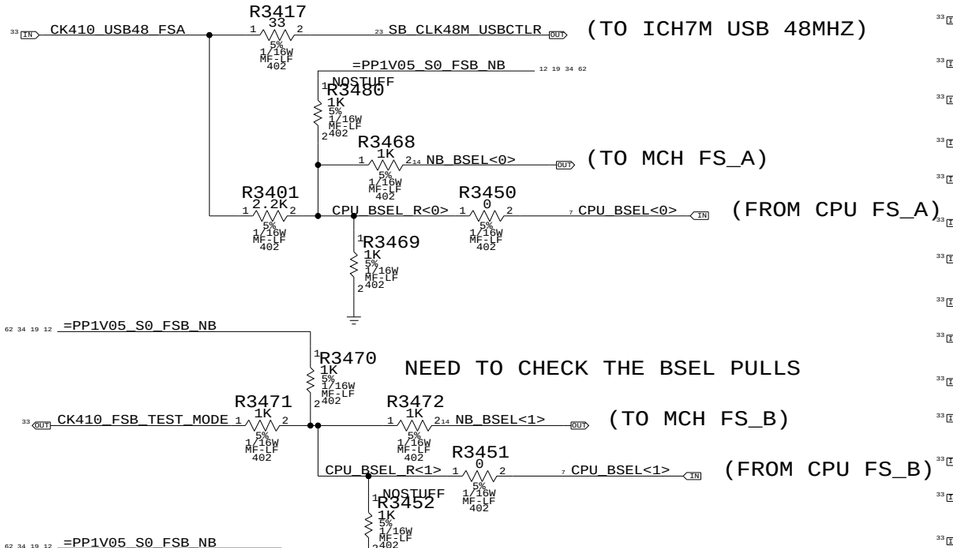
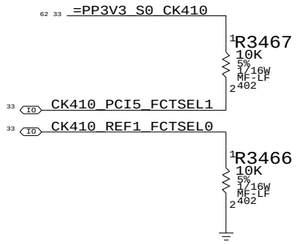


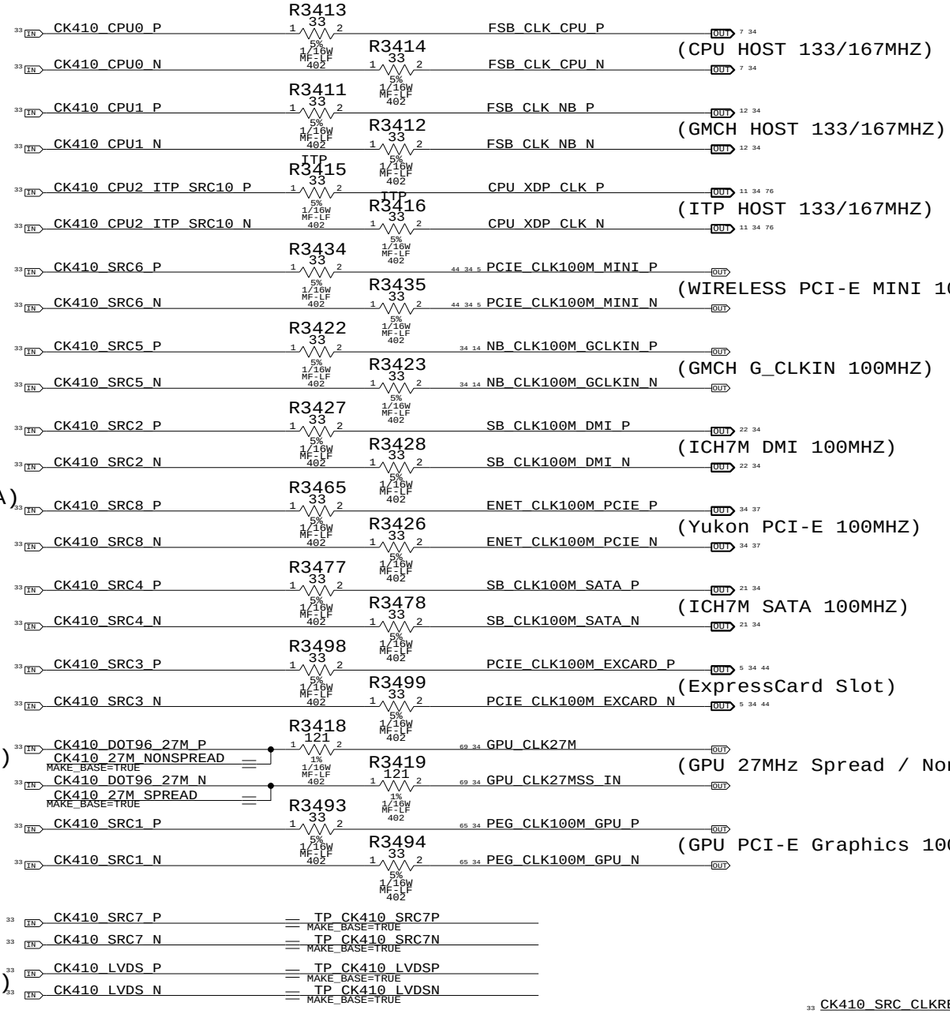


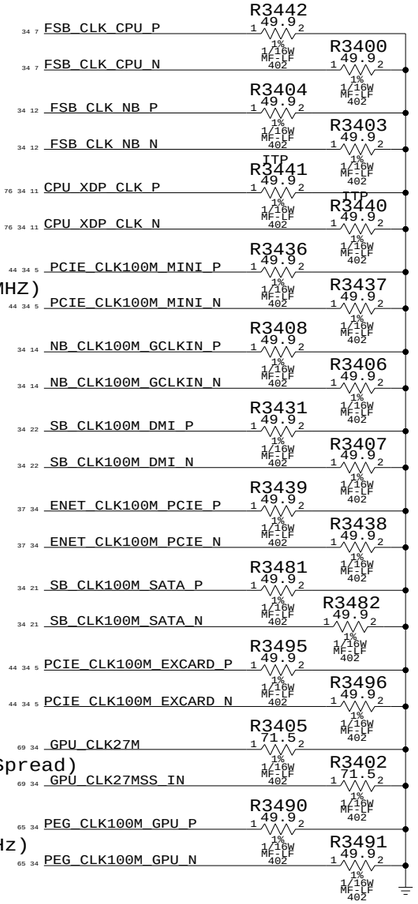


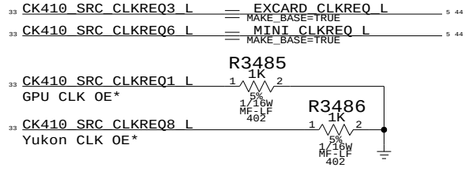
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT: 34	OF: 103

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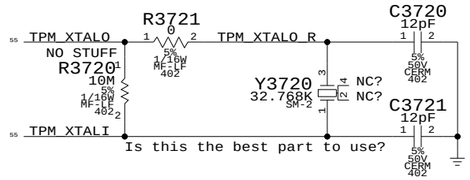
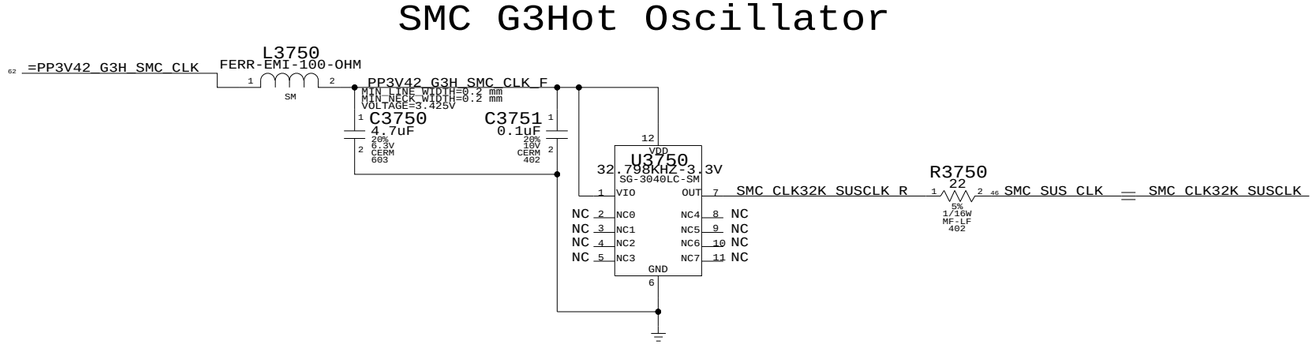
TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE: NONE

SHT 37 OF 103

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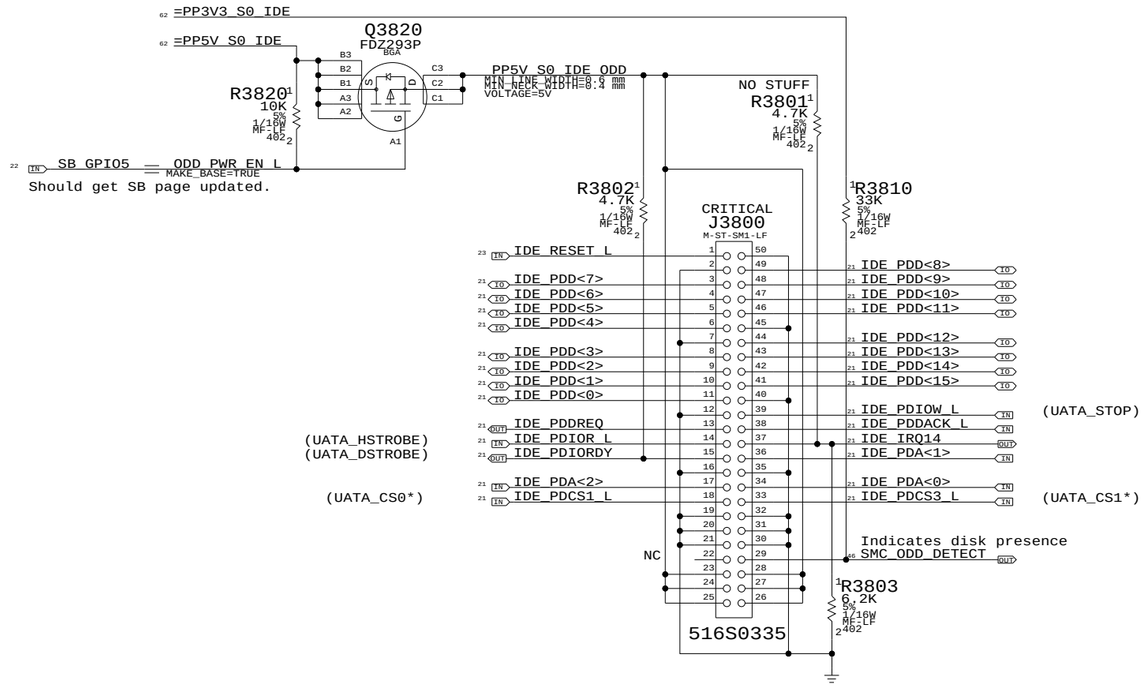
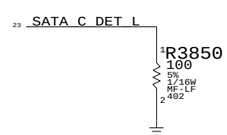
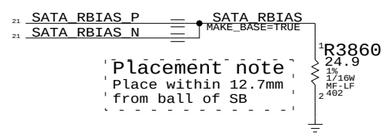
IDE (ODD) Connector





21 SATA_A_R2D_C_P — TP_SATA_A_R2DP
MAKE_BASE=TRUE
21 SATA_A_R2D_C_N — TP_SATA_A_R2DN
MAKE_BASE=TRUE
21 SATA_A_D2R_P — TP_SATA_A_D2RP
MAKE_BASE=TRUE
21 SATA_A_D2R_N — TP_SATA_A_D2RN
MAKE_BASE=TRUE



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	38	103

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PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 120-OHM-0.2A-EMI 0402-LF =PP2V5_S3_ENET 38 62

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET 62 37
=PP1V2_S3_ENET 37 62
=PP3V3_S3_ENET 37 62

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402
C4113 0.1UF 10% 16V X5R 402

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P 22 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 22 PCIE_A_D2R_N OUT
PCIE_A_R2D_P 22 PCIE_A_R2D_C_P IN
PCIE_A_R2D_N 22 PCIE_A_R2D_C_N IN

LEMENU
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

ENET_LOM_DIS_L	10	LOM_DISABLE*	
	12	VAUX_AVLBL	
	47	VMAIN_AVLBL	
NC	11	SWITCH_VCC	
NC	9	SWITCH_VAUX	
NC	24	HSDACP	
NC	25	HSDACN	
OUT 6 ENET_CTRL25	4	CTRL25	
OUT 6 ENET_CTRL12	3	CTRL12	
ENET_RSET	16	RSET	
NC	59	LED_ACT*	
NC	60	LED_LINK10/100*	
NC	62	LED_LINK1000*	
NC	63	LINK*	
	29	TSTPT	
	46	TESTMODE	
	58	VDD7	
	48	VDD6	
	44	VDD5	
	39	VDD4	
	33	VDD3	
	13	VDD2	
	7	VDD1	
	2	VDD0	
	61	VDDO_TTL4	
	45	VDDO_TTL3	
	40	VDDO_TTL2	
	8	VDDO_TTL1	
	1	VDDO_TTL0	
	23	AVDD	
	57	AVDDL6	
	52	AVDDL5	
	51	AVDDL4	
	32	AVDDL3	
	28	AVDDL2	
	22	AVDDL1	
	19	AVDDL0	
	64	VDD25	
	49	TX_P	
	50	TX_N	
PCIE_A_R2D_P	54	RX_P	
PCIE_A_R2D_N	53	RX_N	
	55	REFCLKP	34 ENET_CLK100M_PCIE_P IN
	56	REFCLKN	34 ENET_CLK100M_PCIE_N IN
	6	WAKE*	44 23 5 PCIE_WAKE_L OUT
	5	PERST*	26 ENET_GATED_RST_L IN
	17	MDIP0	38 ENET_MDI_P<0> IO
	18	MDIN0	38 ENET_MDI_N<0> IO
	20	MDIP1	38 ENET_MDI_P<1> IO
	21	MDIN1	38 ENET_MDI_N<1> IO
	26	MDIP2	38 ENET_MDI_P<2> IO
	27	MDIN2	38 ENET_MDI_N<2> IO
	30	MDIP3	38 ENET_MDI_P<3> IO
	31	MDIN3	38 ENET_MDI_N<3> IO
	38	VPD_CLK	ENET_VPD_CLK 37
	41	VPD_DATA	ENET_VPD_DATA 37
	42	PU_VDDO_TTL0	ENET_PU_VDD_TTL0 37
	43	PU_VDDO_TTL1	ENET_PU_VDD_TTL1 37
	35	SPI_DI	NC
	34	SPI_DO	NC
	37	SPI_CLK	NC
	36	SPI_CS	NC
	15	XTALI	ENET_XTALI
	14	XTALO	ENET_XTALO
	67	THRML_PAD	

NO PULL-UP NEEDED

R4102 4.87K 1% 1/16W MF-LF 402

ASF IS UNAVAILABLE ON 8053

INTERNAL PULL-UP

Y4101 25.0000M SM-3

C4150 33PF 5% 50V CERM 402
C4151 33PF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

R4106 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET 37 62

R4130 4.7K 5% 1/16W MF-LF 402 ENET_PU_VDD_TTL0 37
R4131 4.7K 5% 1/16W MF-LF 402 ENET_PU_VDD_TTL1 37

=PP3V3_S3_ENET 62 37

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

U4102 M24C08 SO8

3	E2	
2	NC1	
1	NC0	
7	WC*	
8	VCC	OMIT
5	SDA	ENET_VPD_DATA 37
6	SCL	ENET_VPD_CLK 37
4	VSS	

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP1V2_S3_ENET 62 37

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP3V3_S3_ENET 62 37

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

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NONE	41	103

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

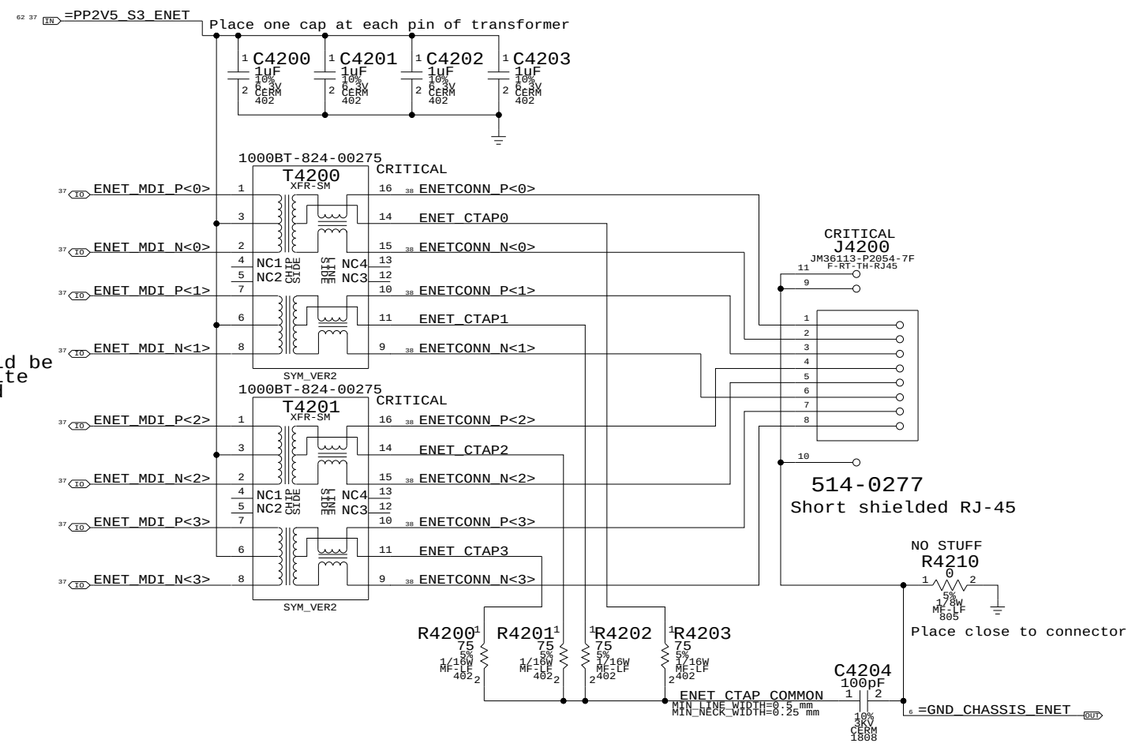
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

SCALE	SHT	OF
NONE	42	103

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PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23256 ADDED
6/21/2005 - CHANGED INT_PIRQD_L TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IDSEL TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP

=PP3V3_S0_FW

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V X5R 402
C4422 0.1UF 10% 10V CERM 402
C4426 0.1UF 10% 10V X5R 402
C4428 0.1UF 10% 10V CERM 402
C4430 0.1UF 10% 10V X5R 402
C4432 0.1UF 10% 10V CERM 402

L4400 600-OHM-300MA 0402

PP3V3_S0_FW_AVDD

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

=PP3V3_S0_PCI

CONNECT TO VDD FOR 3.3V OPERATION

U4400
FW32306
BGA
LEMENU

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF 402

THIS IS FROM ICH-7M

197S0030 3.2MMX2.5MM

Y4403 SM 24.576MHZ

R4400 390 1% 1/16W MF 402

C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

R4452 2.49K 1% 1/16W MF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/16W MF 402

SPEC RECOMMENDS 2.49K

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0
TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0 — DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’) SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

MANUFACTURING TEST PINS

TEST0	C2
TEST1	C1
PHYTEST	A4
SE	A3
SM	B3

FIREWIRE CONTROLLER

SYNC_MASTER=MSX SYNC_DATE=07/26/2005

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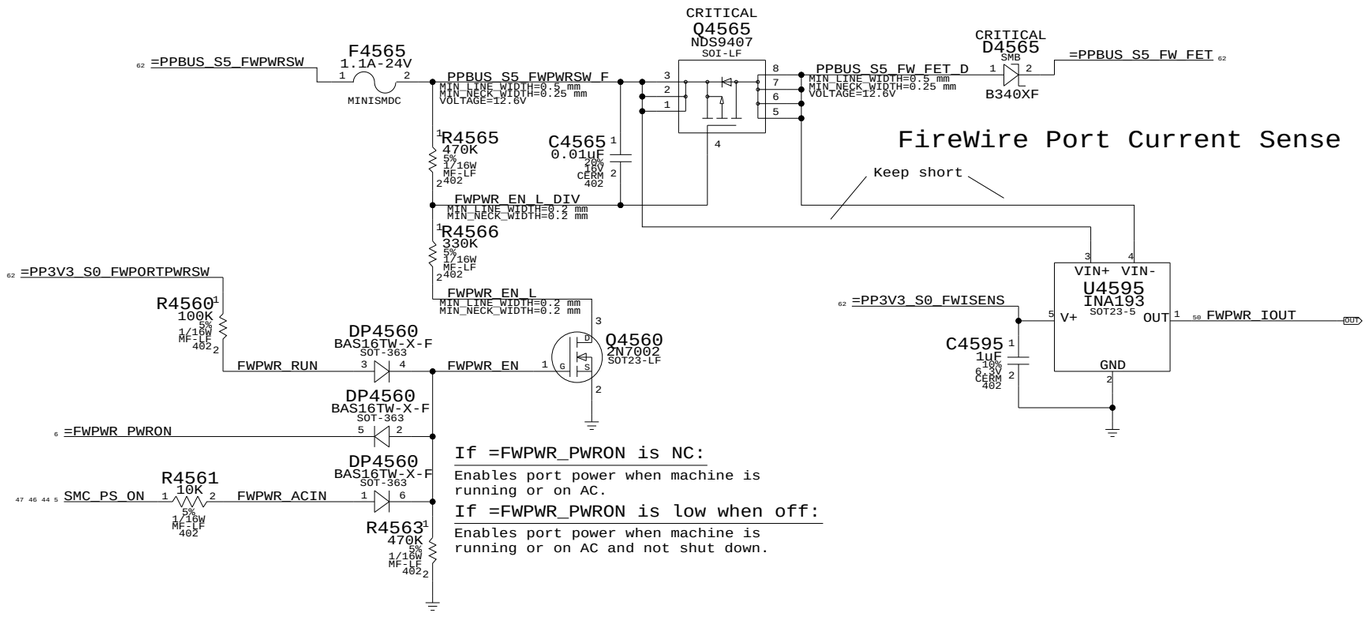
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

SCALE	SHT	OF
NONE	45	103

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_FW
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

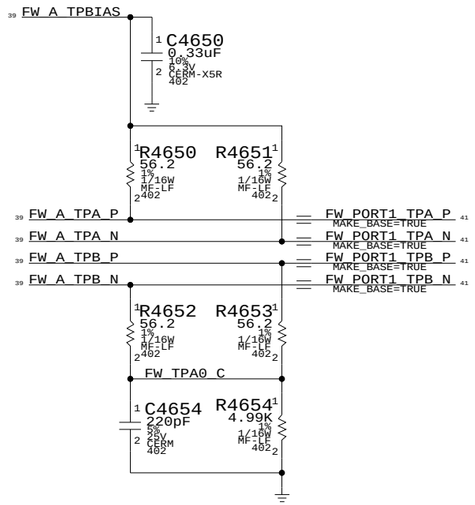
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

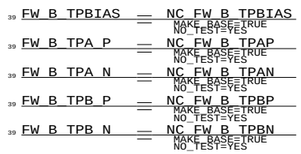
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

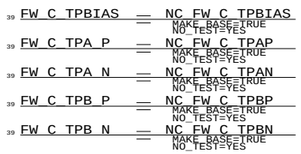
Place close to FireWire PHY



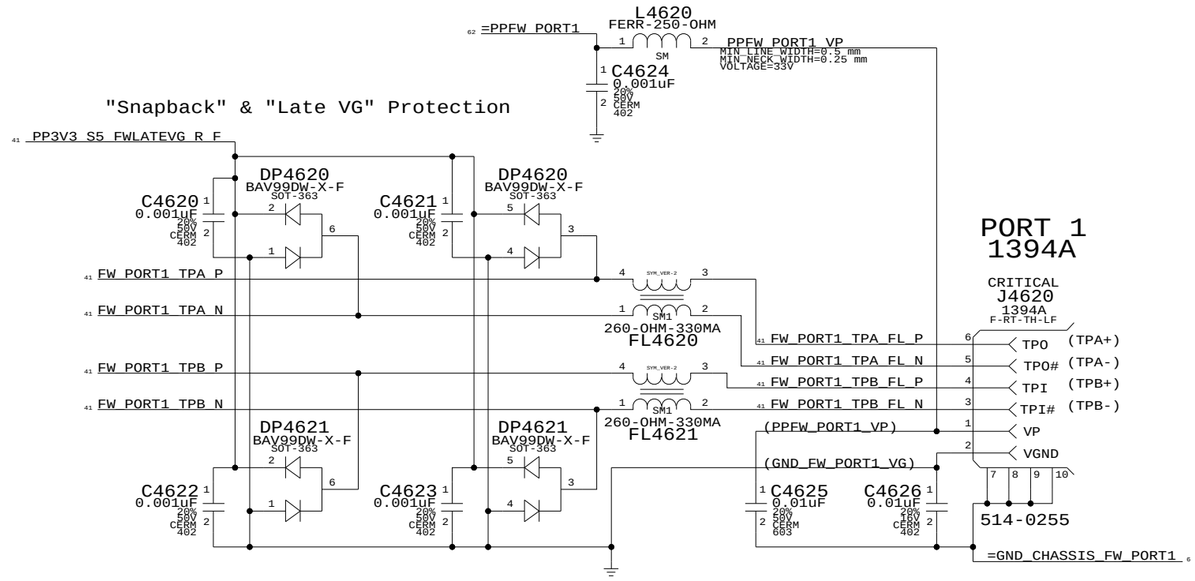
2nd TPA/TPB pair unused

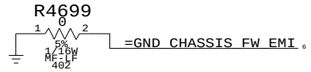

39 FW_B_TPBIAS = NC_FW_B_TPBIAS MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPA_P = NC_FW_B_TPAP MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPA_N = NC_FW_B_TPAN MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPB_P = NC_FW_B_TPBP MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPB_N = NC_FW_B_TPBN MAKE_BASE=TRUE NO_TEST=YES

3rd TPA/TPB pair unused

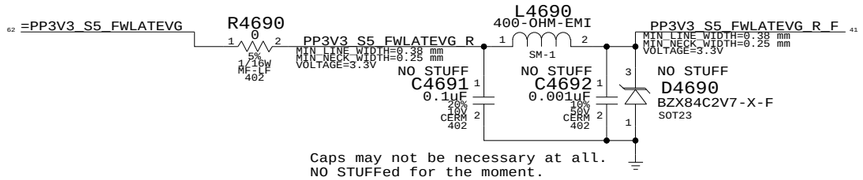

39 FW_C_TPBIAS = NC_FW_C_TPBIAS MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPA_P = NC_FW_C_TPAP MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPA_N = NC_FW_C_TPAN MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPB_P = NC_FW_C_TPBP MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPB_N = NC_FW_C_TPBN MAKE_BASE=TRUE NO_TEST=YES

Cable Power





Late-VG Protection Power


62 =PP3V3_S5_FWLATEVG
R4690 0 5% 1/16W MF-LF 402
PP3V3_S5_FWLATEVG_R MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
L4690 400-OHM-EMI SM-1
PP3V3_S5_FWLATEVG_R_F 41 MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
NO STUFF C4691 0.1uF 20% 10V CERM 402
NO STUFF C4692 0.001uF 10% 50V CERM 402
NO STUFF D4690 BZX84C2V7-X-F SOT23
Caps may not be necessary at all.
NO STUFFed for the moment.

FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03
SCALE: NONE	SHT 46 OF 103	

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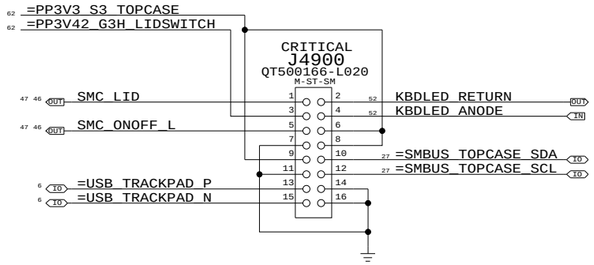
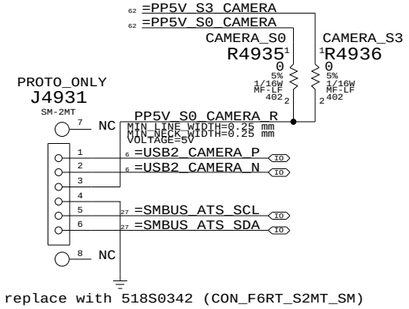
Top-Case Connector

(Pinout is almost fixed)

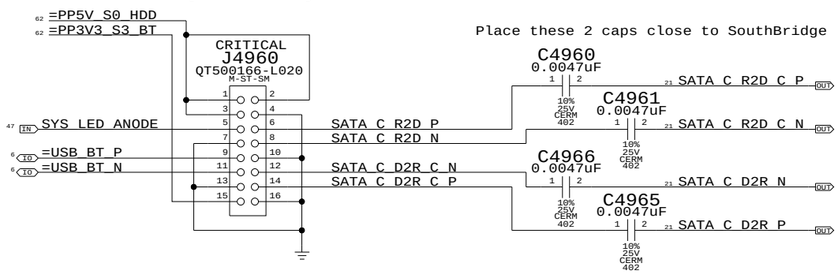


Camera Connector



Post-proto, replace with 518S0342 (CON_F6RT_S2MT_SM)

Bluetooth (M13P) & SATA HDD Flex Connector



Internal USB Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	49	103

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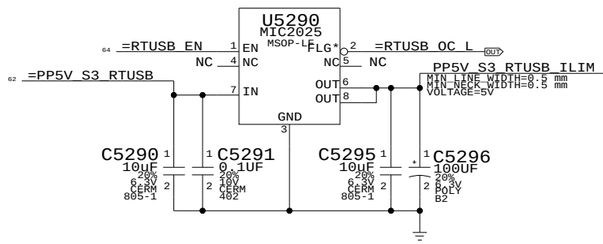
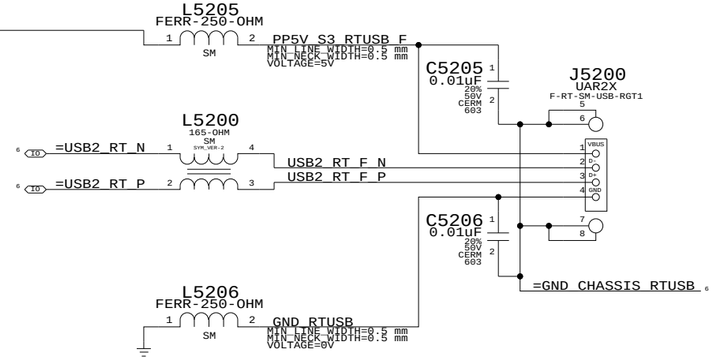
Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

SCALE	SHT	OF
NONE	52	103

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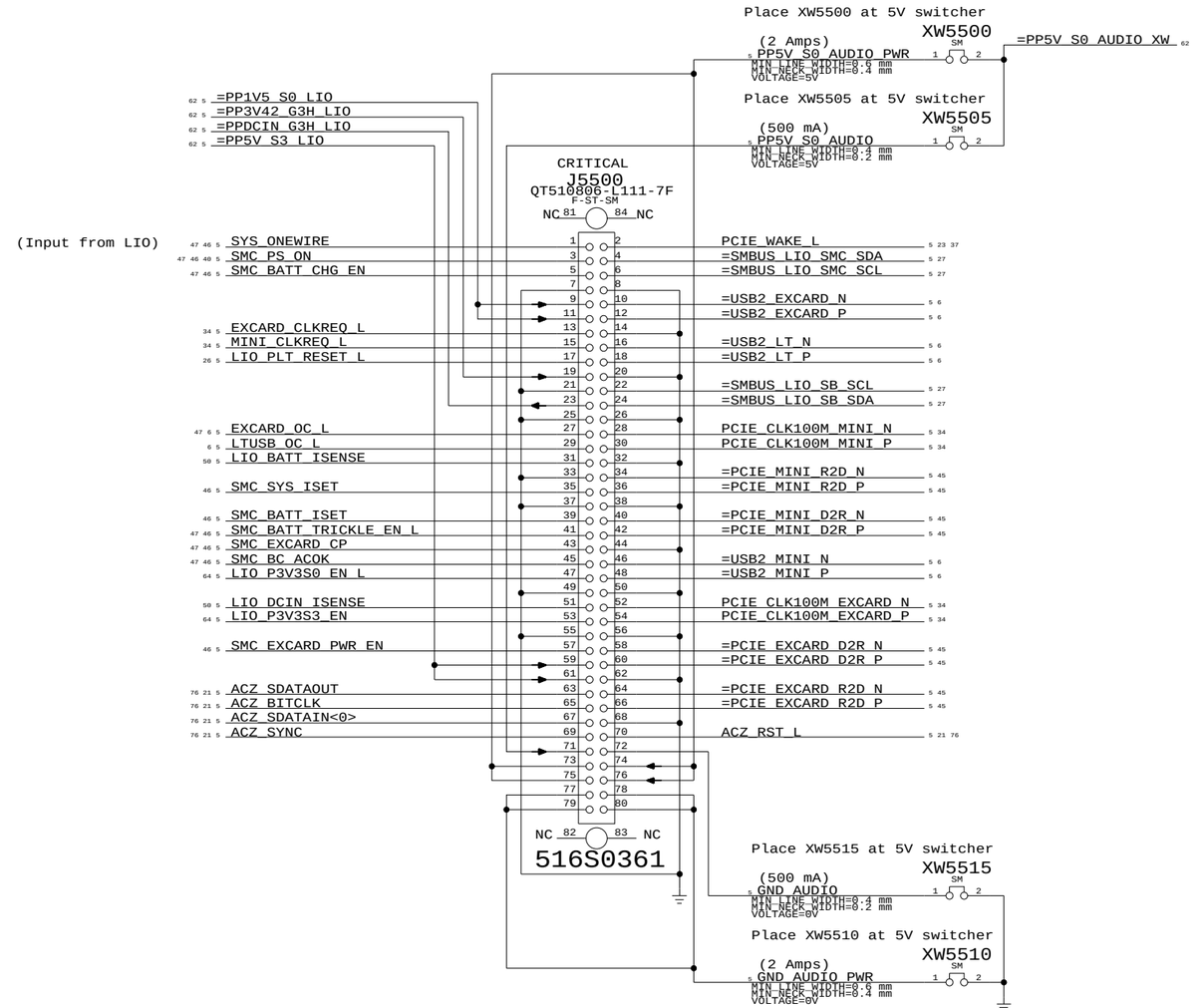
Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	55	103

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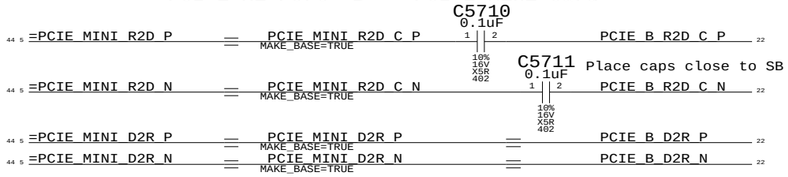
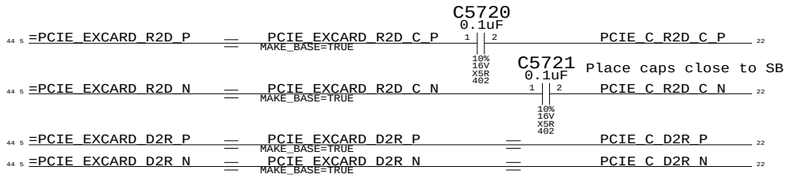
PCI-E x1 Port "A" = Ethernet (Yukon)

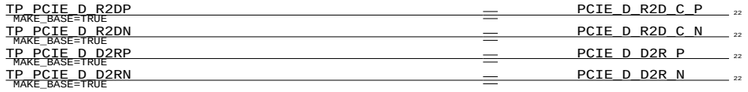
PCI-E x1 Port "B" = PCI-E Mini Card



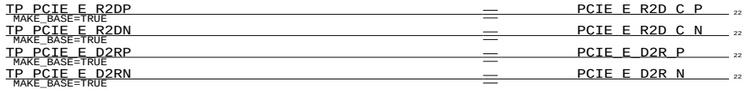
PCI-E x1 Port "C" = ExpressCard



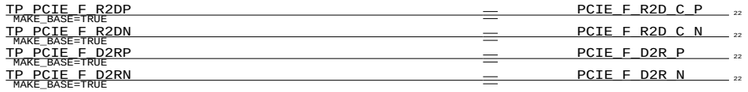
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

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NONE	57	103

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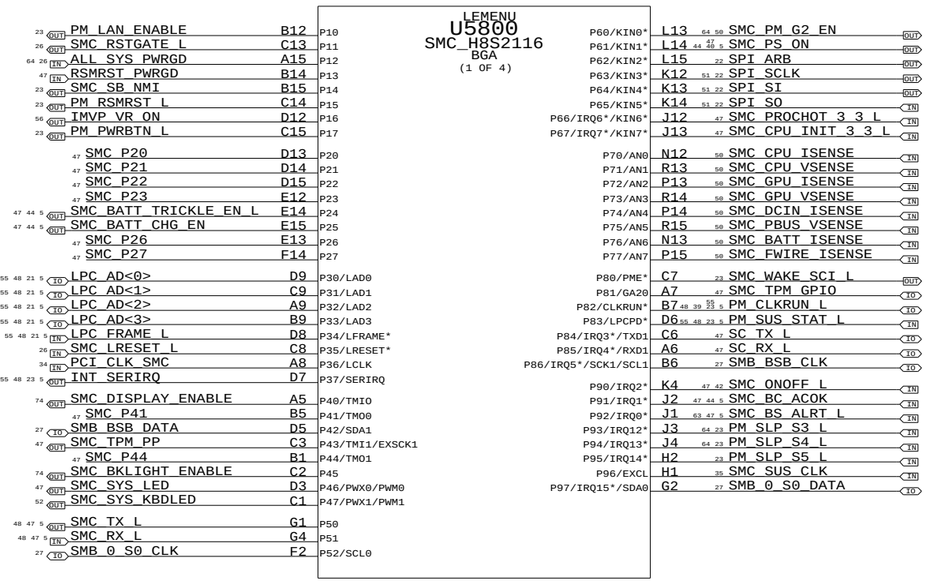

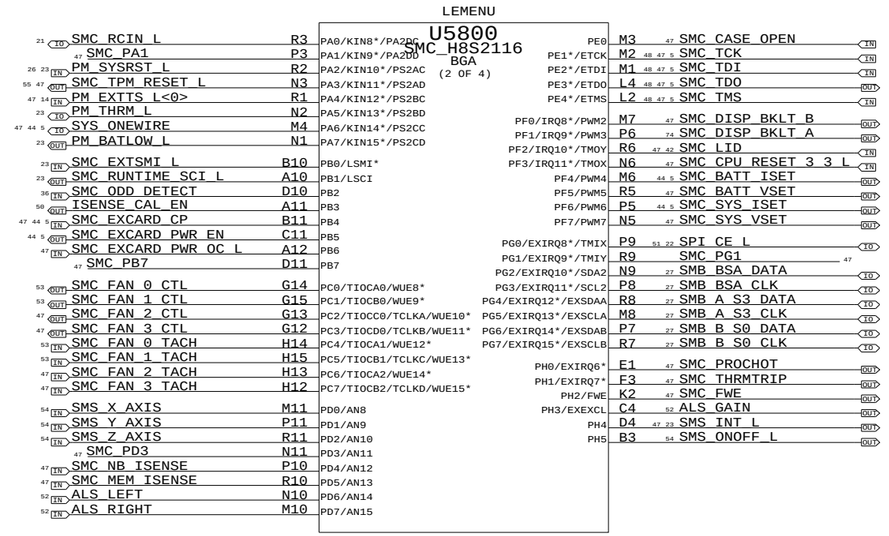

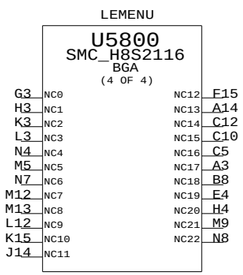

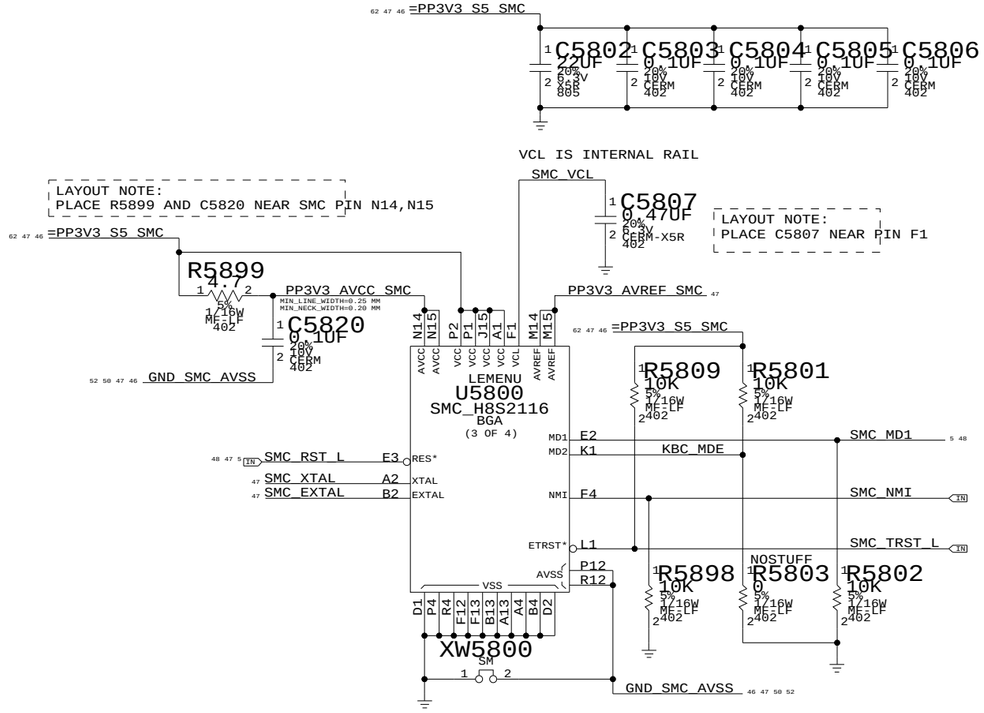

SMC

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SCALE	SHT	OF
NONE	58	103

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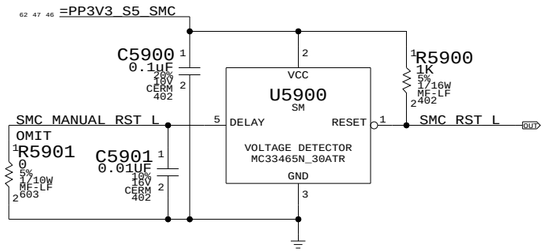
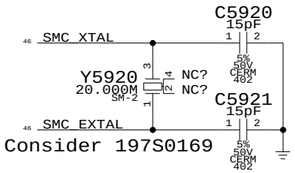
SMC Reset Button / Brownout Detect



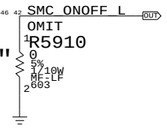
Silk: "SMC RST"

SMC Crystal Circuit



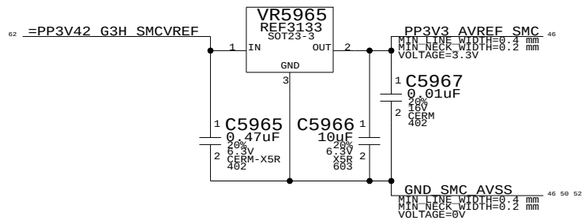
Post-Proto: Consider 197S0169

Debug Power Button

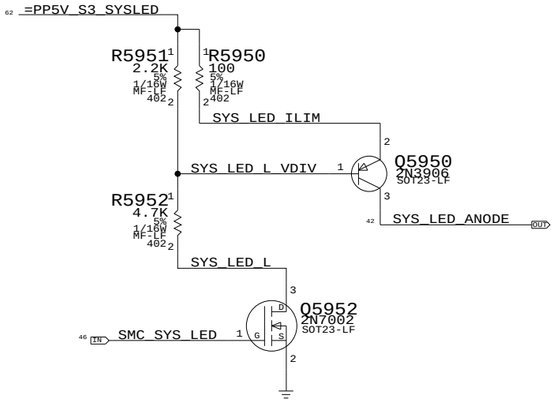


Silk: "PWR BTN"

SMC AVREF Supply

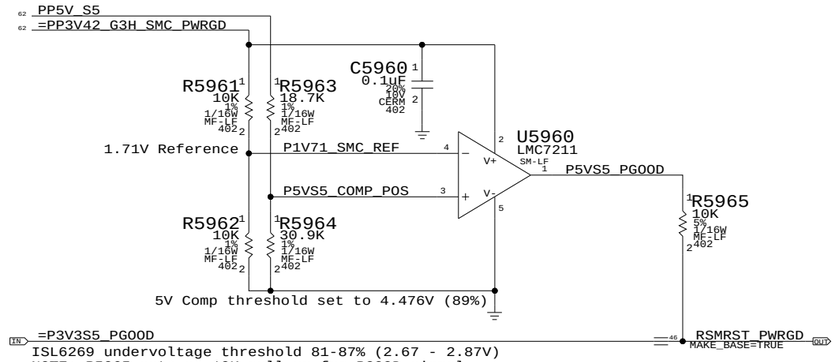


System (Sleep) LED Circuit

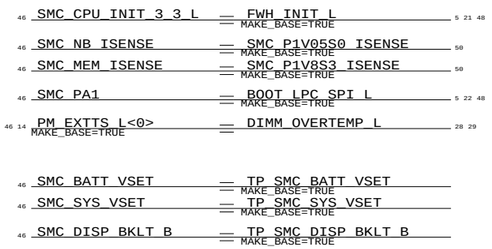


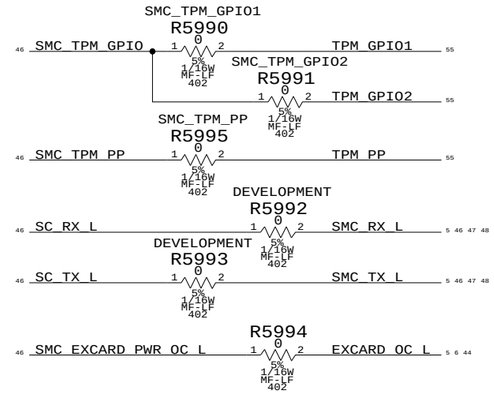
SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

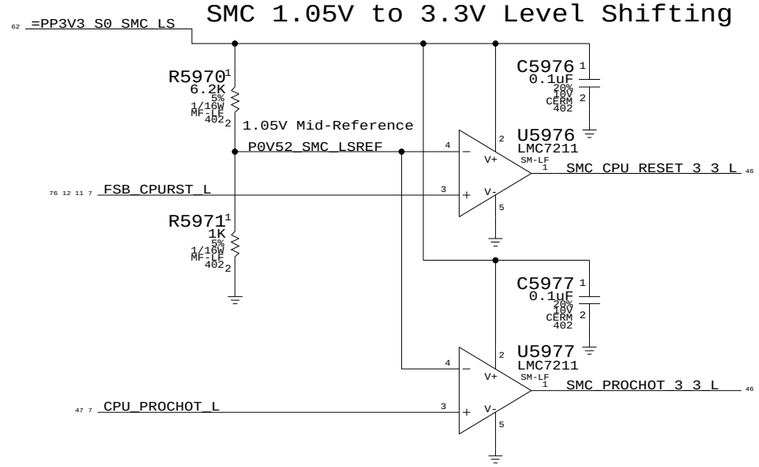


ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

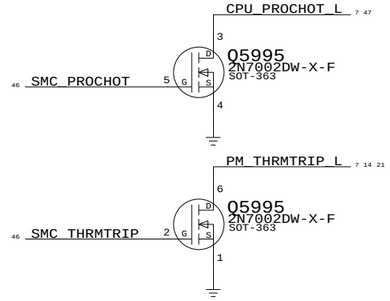

46 SMC_CPU_INIT_3_3_L — FWH_INIT_L 5 21 48
46 SMC_NB_ISENSE — SMC_P1V05S0_ISENSE 50
46 SMC_MEM_ISENSE — SMC_P1V8S3_ISENSE 50
46 SMC_PA1 — BOOT_LPC_SPI_L 5 22 48
46 14 PM_EXTTS_L<0> — DIMM_OVERTEMP_L 28 29
MAKE_BASE=TRUE
46 SMC_BATT_VSET — TP_SMC_BATT_VSET
46 SMC_SYS_VSET — TP_SMC_SYS_VSET
46 SMC_DISP_BKLT_B — TP_SMC_DISP_BKLT_B
46 SMC_FAN_2_CTL — TP_SMC_FAN_2_CTL
46 SMC_FAN_2_TACH — TP_SMC_FAN_2_TACH
46 SMC_FAN_3_CTL — TP_SMC_FAN_3_CTL
46 SMC_FAN_3_TACH — TP_SMC_FAN_3_TACH
SMC_P20 — TP_SMC_P20
46 SMC_P21 — TP_SMC_P21
46 SMC_P22 — TP_SMC_P22
46 SMC_P23 — TP_SMC_P23
46 SMC_P26 — TP_SMC_P26
46 SMC_P27 — TP_SMC_P27
46 SMC_P41 — TP_SMC_P41
46 SMC_P44 — TP_SMC_P44
46 SMC_PB7 — TP_SMC_PB7
46 SMC_PD3 — TP_SMC_PD3
46 SMC_PG1 — TP_SMC_PG1
MAKE_BASE=TRUE

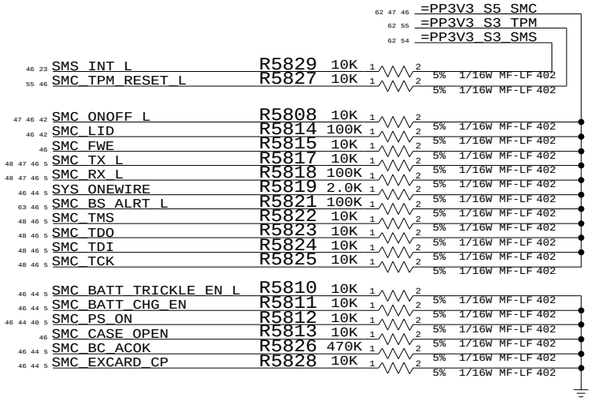


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

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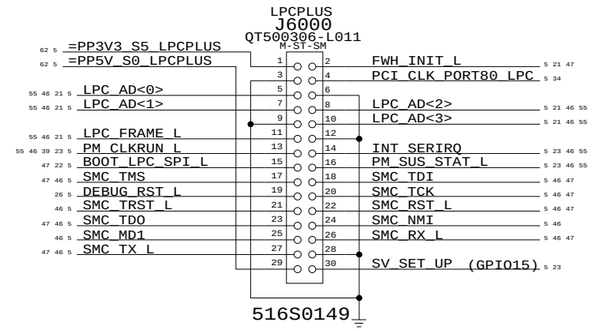
LPCPLUS
J6000
QT500306-L011
M-ST-SM
62 5 =PP3V3_S5_LPCPLUS
62 5 =PP5V_S0_LPCPLUS
55 46 21 5 LPC_AD<0>
55 46 21 5 LPC_AD<1>
55 46 21 5 LPC_FRAME_L
55 46 39 23 5 PM_CLKRUN_L
47 22 5 BOOT_LPC_SPI_L
47 46 5 SMC_TMS
26 5 DEBUG_RST_L
46 5 SMC_TRST_L
47 46 5 SMC_TDO
46 5 SMC_MD1
47 46 5 SMC_TX_L
1 2 FWH_INIT_L 5 21 47
3 4 PCI_CLK_PORT80_LPC 5 34
5 6
7 8 LPC_AD<2> 5 21 46 55
9 10 LPC_AD<3> 5 21 46 55
11 12
13 14 INT_SERIRQ 5 23 46 55
15 16 PM_SUS_STAT_L 5 23 46 55
17 18 SMC_TDI 5 46 47
19 20 SMC_TCK 5 46 47
21 22 SMC_RST_L 5 46 47
23 24 SMC_NMI 5 46
25 26 SMC_RX_L 5 46 47
27 28
29 30 SV_SET_UP (GPIO15) 5 23
516S0149

LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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SCALE	SHT	OF
NONE	60	103

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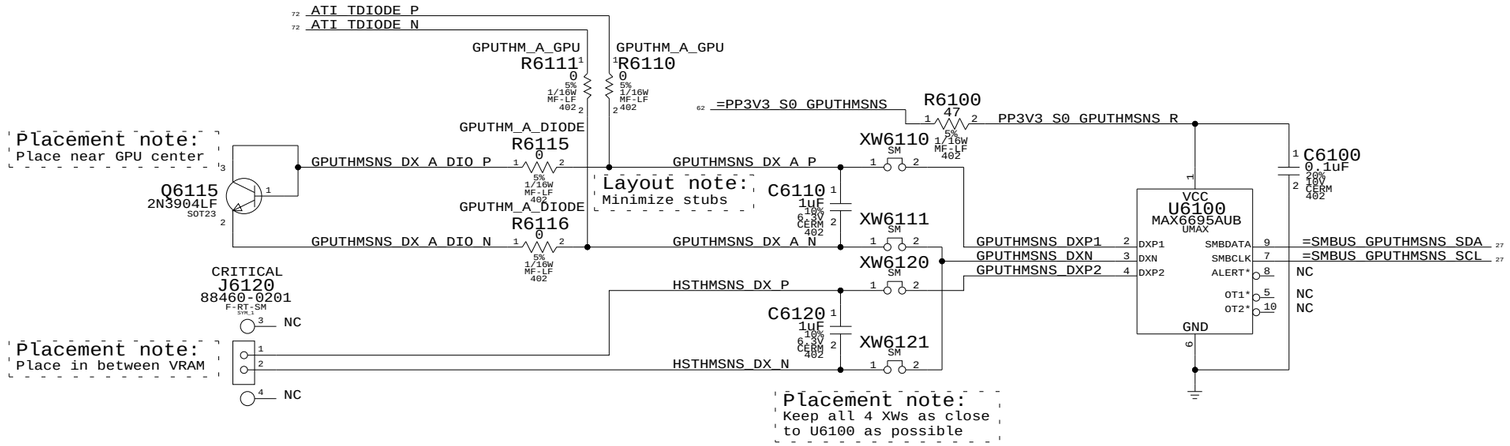
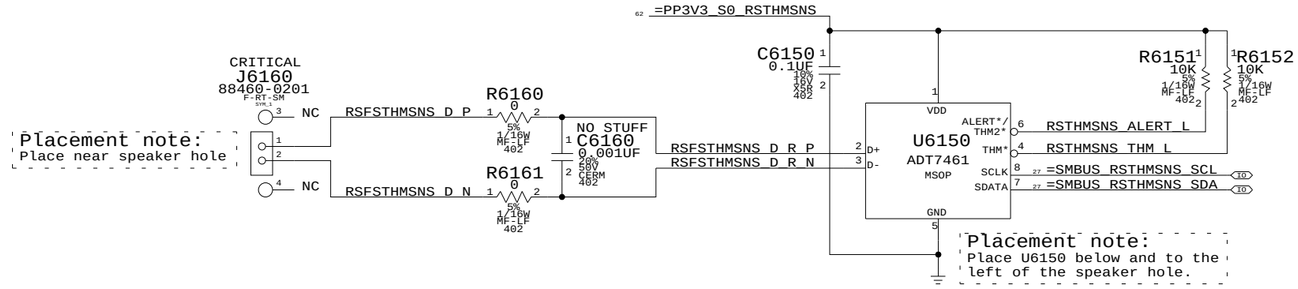
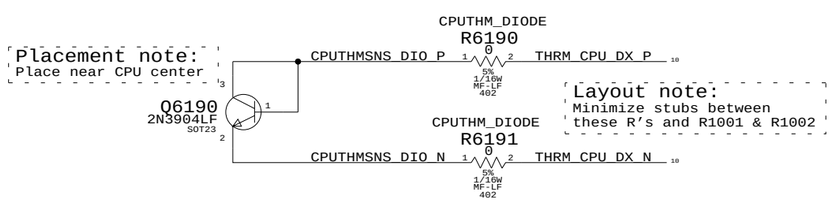
GPU / Heat Pipe Thermal Sensor



Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

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SCALE	SHT	OF
NONE	61	103

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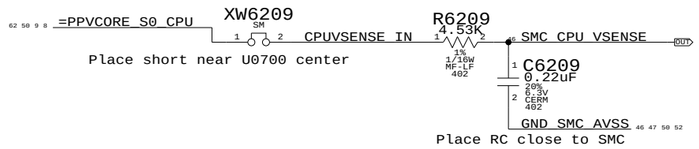
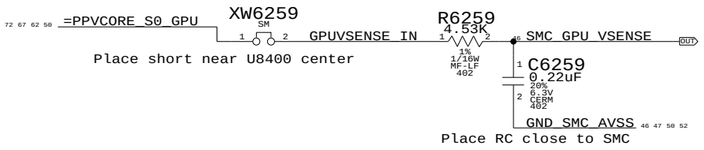
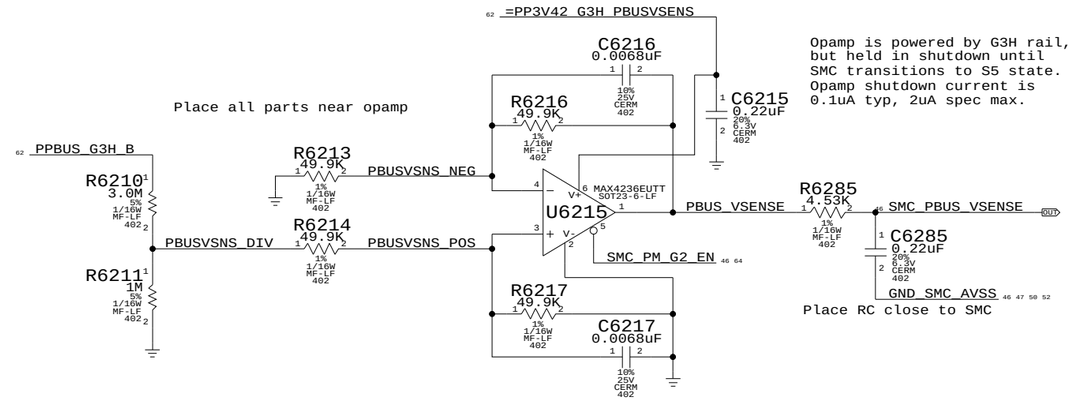
CPU Voltage Sense / Filter



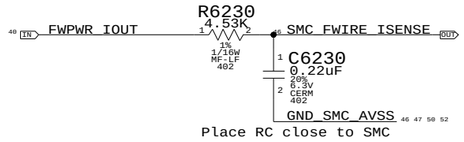
GPU Voltage Sense / Filter



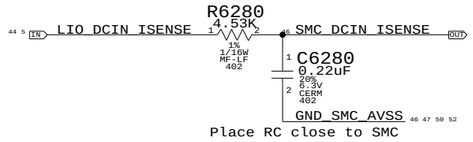
PBUS Voltage Sense Buffer & Filter


62 =PP3V42_G3H_PBUSVSENS
Opamp is powered by G3H rail, but held in shutdown until SMC transitions to S5 state. Opamp shutdown current is 0.1uA typ, 2uA spec max.
Place all parts near opamp
62 PPBUS_G3H_B
R6210 3.0M 5% 1/16W MF-LF 402
R6211 1M 5% 1/16W MF-LF 402
PBUSVSNS_DIV
R6213 49.9K 1% 1/16W MF-LF 402
R6214 49.9K 1% 1/16W MF-LF 402
PBUSVSNS_NEG
PBUSVSNS_POS
C6216 0.0068UF 10% 25V CERM 402
C6215 0.22uF 20% 6.3V CERM 402
R6216 49.9K 1% 1/16W MF-LF 402
R6217 49.9K 1% 1/16W MF-LF 402
C6217 0.0068UF 10% 25V CERM 402
U6215
MAX4236EUTT SOT23-6-LF
PBUS_VSENSE
SMC_PM_G2_EN 46 64
R6285 4.53K 1% 1/16W MF-LF 402
SMC_PBUS_VSENSE
C6285 0.22uF 20% 6.3V CERM 402
GND_SMC_AVSS 46 47 50 52
Place RC close to SMC

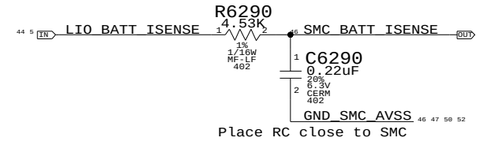
FireWire Current Sense Filter



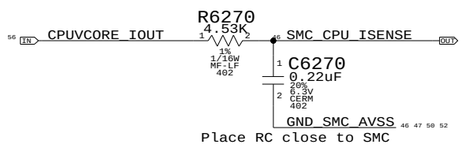
DCIN Current Sense Filter



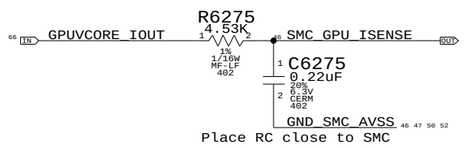
Battery Current Sense Filter



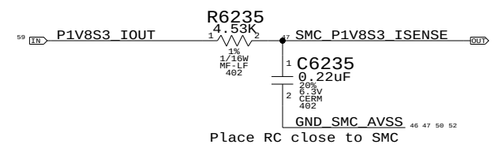
CPU Current Sense Filter



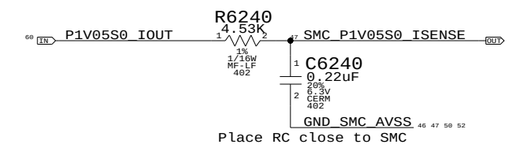
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

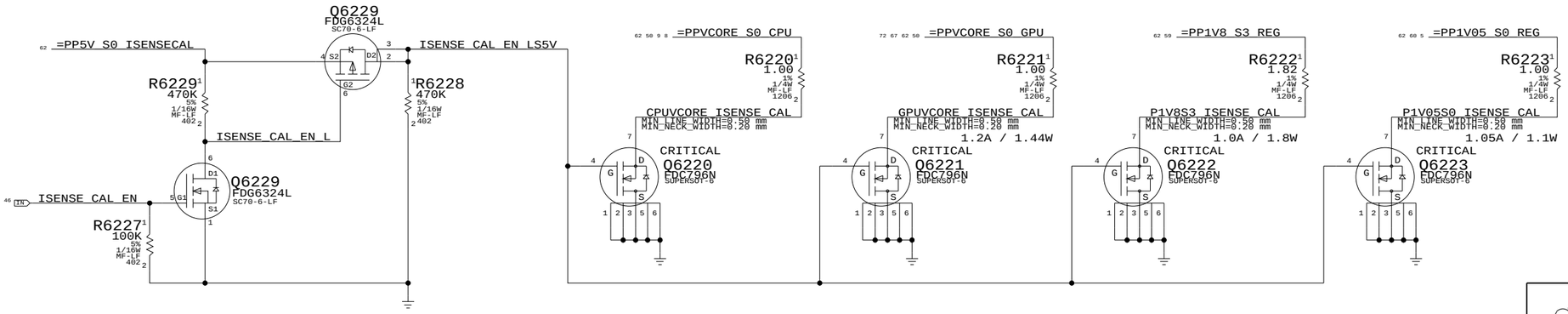


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

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NONE	62	103

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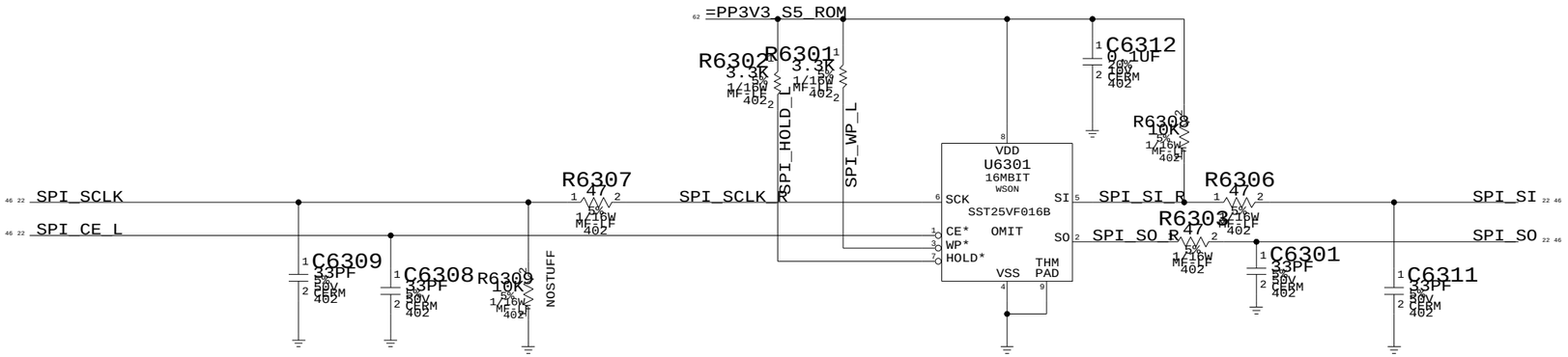
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0384	1	IC,16MBIT -PIN SPI SERIAL FLASH,SOIC8	U6301		LEMENU



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MSZ SYNC_DATE=07/26/2005

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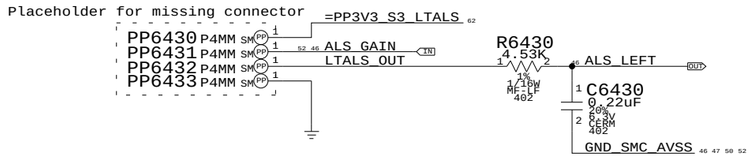
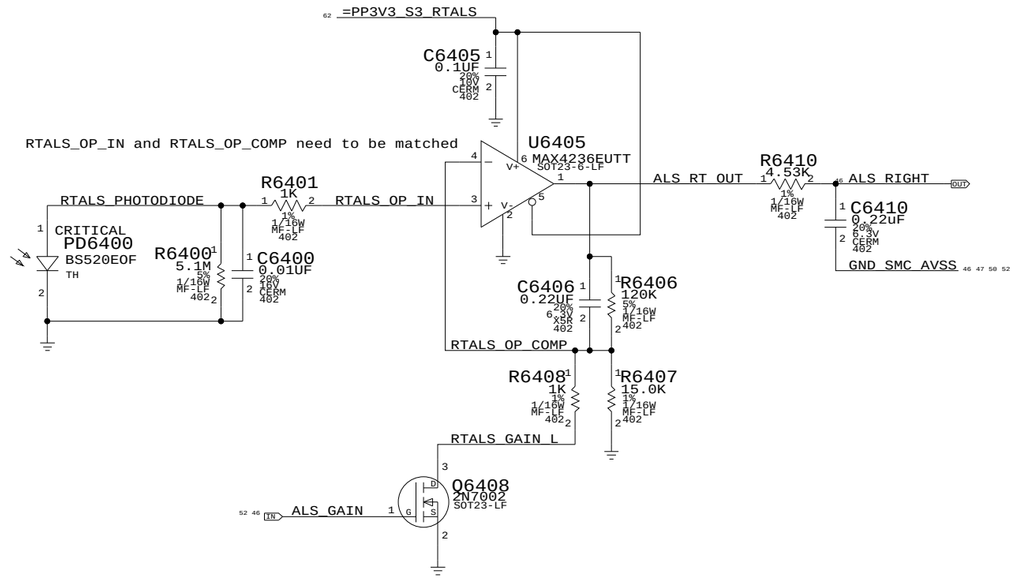
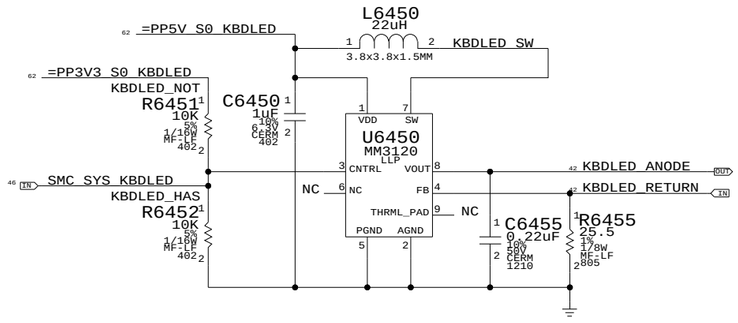
Left ALS "Connector"



Right ALS Circuit



Keyboard LED Driver



ALS Support

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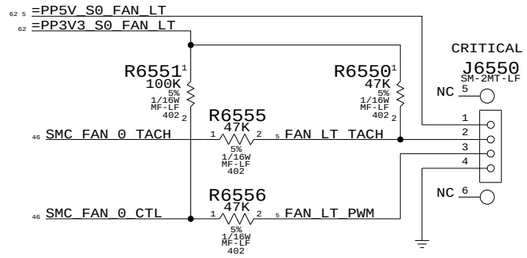
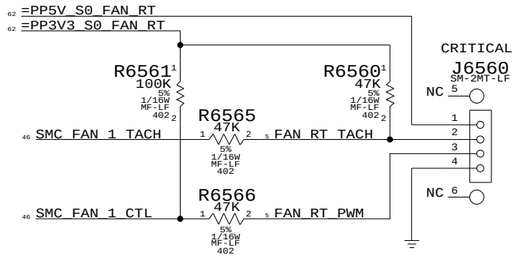
Left Fan



Right Fan



Fan Connectors

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PAGE NOTES

INPUT

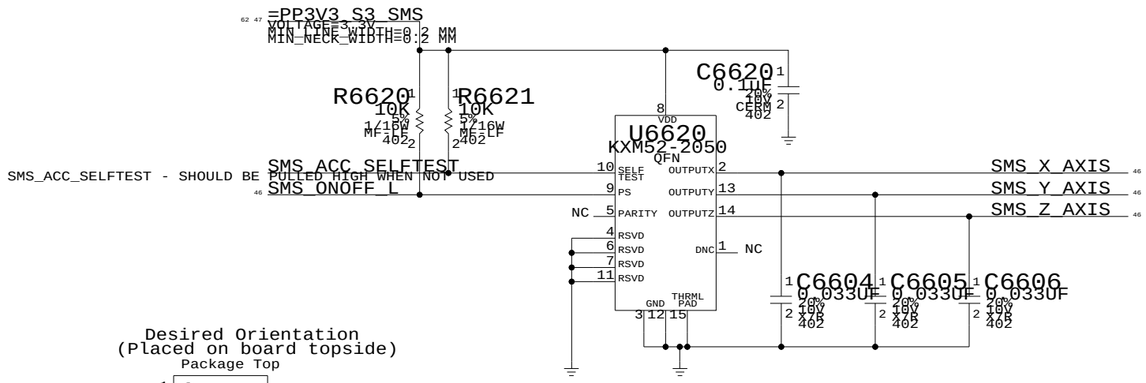
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

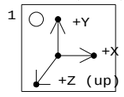
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



Desired Orientation
(Placed on board topside)
Package Top



SMS
SYNC_MASTER=MSY SYNC_DATE=07/26/2005

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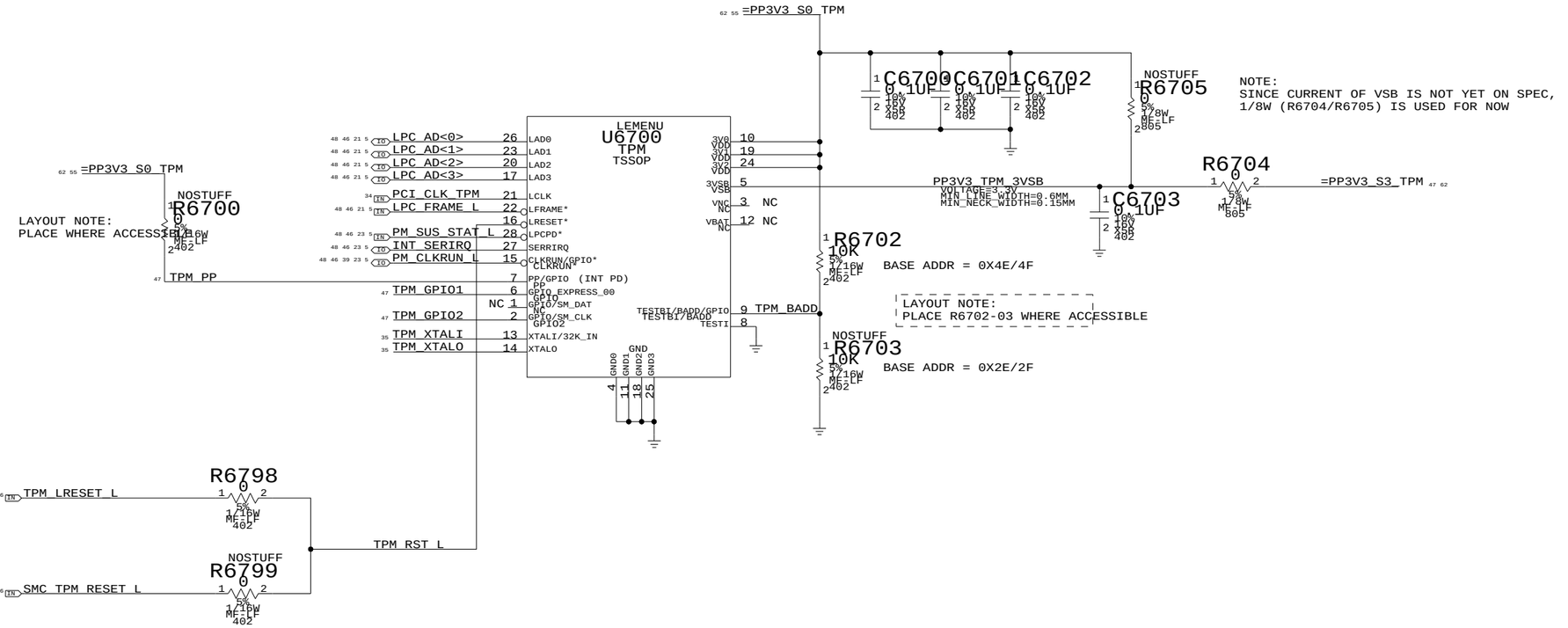

TPM

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NONE	67	103

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DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

Placement Note:
Keep R7599 and R7596 close to inductor

IMVP6 CPU VCore Regulator

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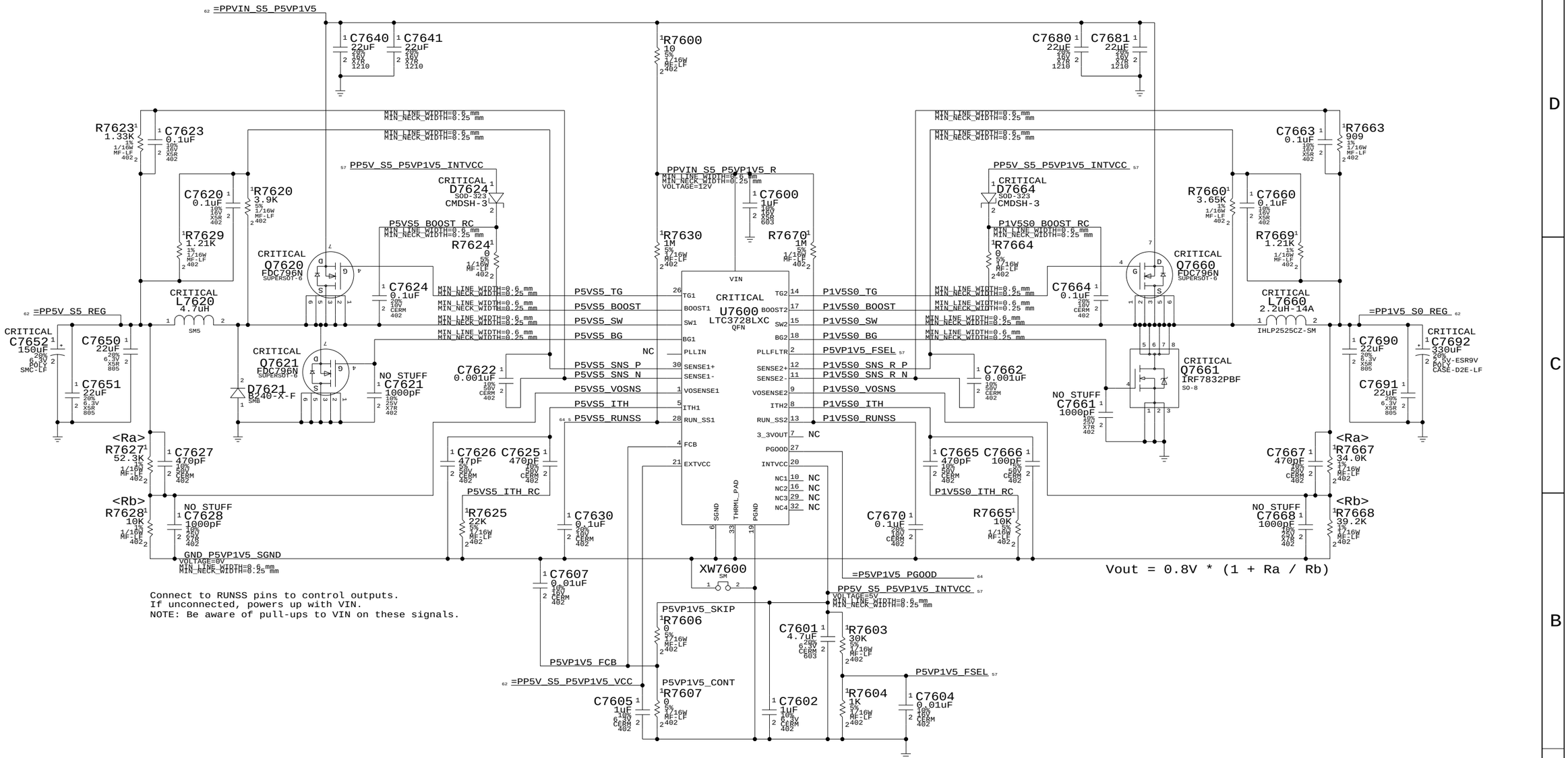

5V / 1.5V Power Supply

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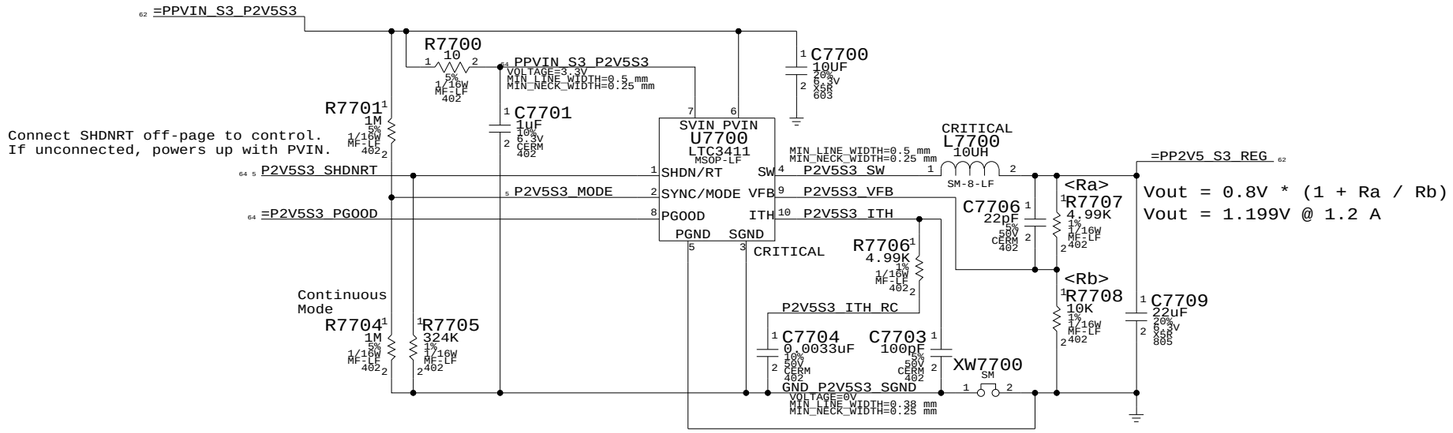
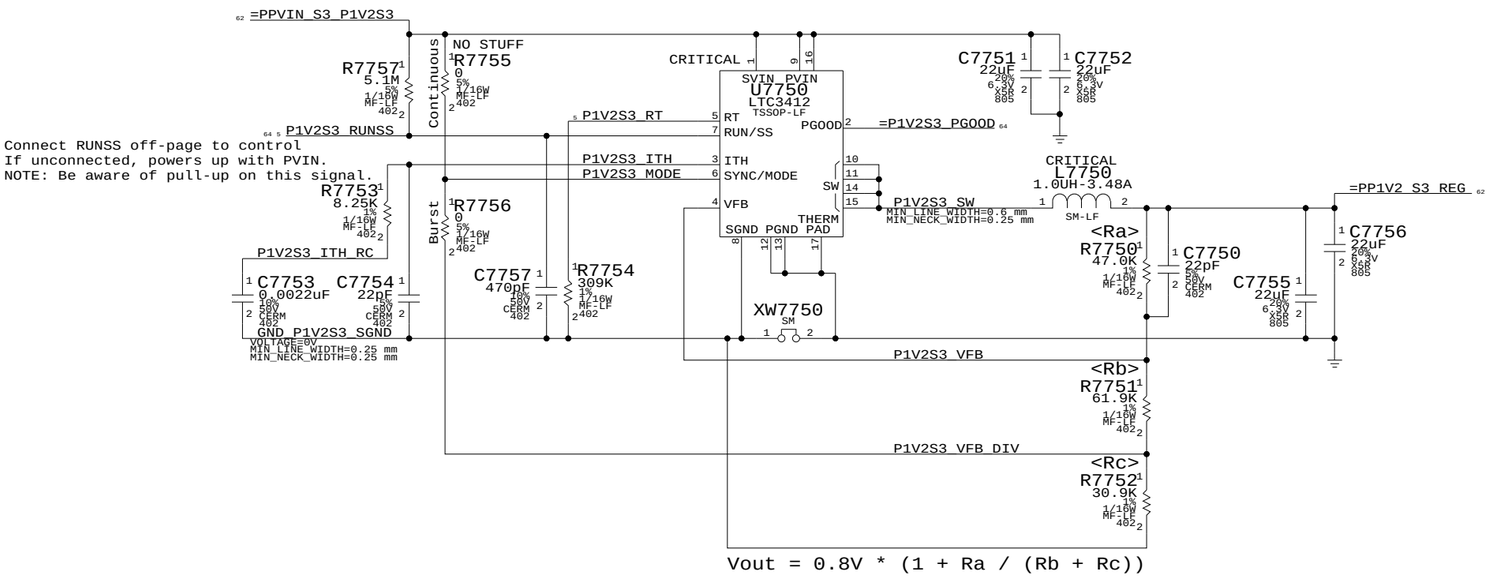
2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

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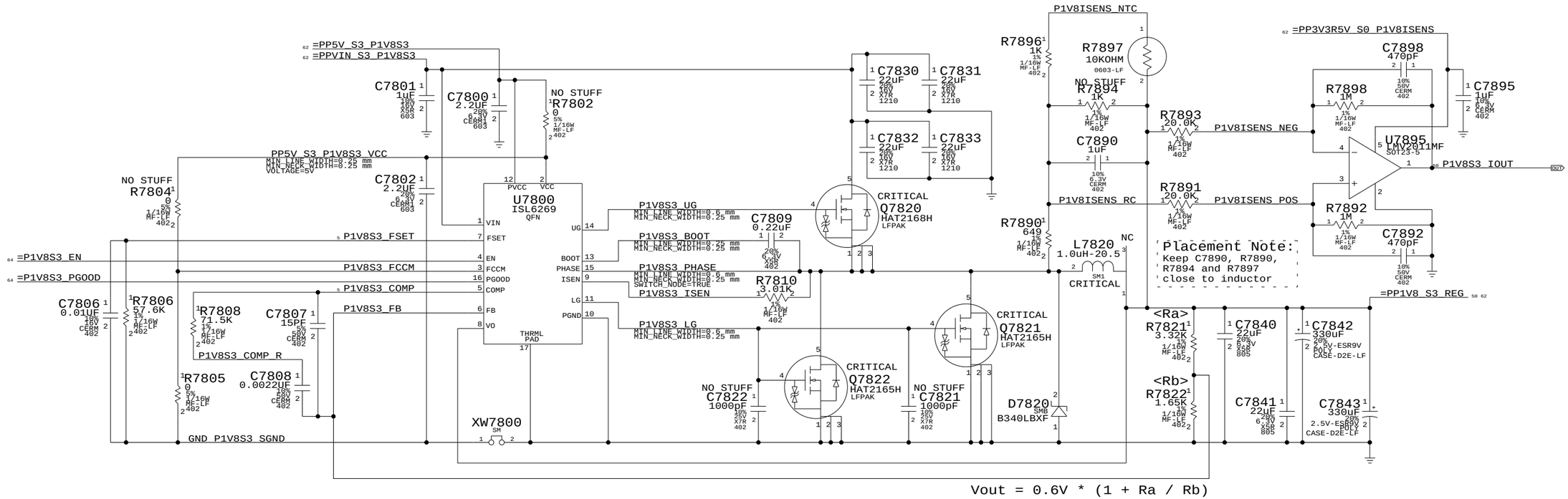
1.8V S3 Current Sense


=PP5V_S3_P1V8S3
=PPVIN_S3_P1V8S3
C7801 1uF 10V X5R 603
C7800 2.2UF 20% 6.3V CERM 603
NO STUFF R7802 0 5% 1/16W MF-LF 402
PP5V_S3_P1V8S3_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C7802 2.2UF 20% 6.3V CERM 603
NO STUFF R7804 0 5% 1/10W MF-LF 402
U7800 ISL6269 QFN
PVCC VCC VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
=P1V8S3_EN
=P1V8S3_PGOOD
P1V8S3_FSET
P1V8S3_FCCM
P1V8S3_COMP
P1V8S3_FB
P1V8S3_COMP_R
C7806 0.01UF 10% 16V CERM 402
R7806 57.6K 1% 1/16W MF-LF 402
R7808 71.5K 1% 1/16W MF-LF 402
C7807 15PF 5% 50V CERM 402
R7805 0 5% 1/16W MF-LF 402
C7808 0.0022UF 10% 50V CERM 402
GND_P1V8S3_SGND
XW7800 SM
P1V8S3_UG
P1V8S3_BOOT
P1V8S3_PHASE
P1V8S3_ISEN
P1V8S3_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
C7809 0.22uF 20% 6.3V X5R 402
R7810 3.01K 1% 1/16W MF-LF 402
C7830 22uF 20% 16V X7R 1210
C7831 22uF 20% 16V X7R 1210
C7832 22uF 20% 16V X7R 1210
C7833 22uF 20% 16V X7R 1210
CRITICAL Q7820 HAT2168H LFPAK
CRITICAL Q7821 HAT2165H LFPAK
CRITICAL Q7822 HAT2165H LFPAK
NO STUFF C7822 1000pF 10% 25V X7R 402
NO STUFF C7821 1000pF 10% 25V X7R 402
D7820 SMB B340LBXF
P1V8ISENS_NTC
R7896 1K 1% 1/10W MF-LF 402
R7897 10KOHM 0603-LF
NO STUFF R7894 1K 1% 1/10W MF-LF 402
C7890 1uF 10% 6.3V CERM 402
R7890 649 1% 1/10W MF-LF 402
L7820 1.0uH-20.5 SM1 CRITICAL
NC
R7893 20.0K 1% 1/10W MF-LF 402
P1V8ISENS_NEG
R7891 20.0K 1% 1/10W MF-LF 402
P1V8ISENS_RC
P1V8ISENS_POS
=PP3V3R5V_S0_P1V8ISENS
C7898 470pF 10% 50V CERM 402
R7898 1M 1% 1/10W MF-LF 402
C7895 1uF 10% 6.3V CERM 402
U7895 LMV2011MF SOT23-5
P1V8S3_IOUT
R7892 1M 1% 1/10W MF-LF 402
C7892 470pF 10% 50V CERM 402
Placement Note: Keep C7890, R7890, R7894 and R7897 close to inductor
=PP1V8_S3_REG
<Ra> R7821 3.32K 1% 1/10W MF-LF 402
<Rb> R7822 1.65K 1% 1/10W MF-LF 402
C7840 22uF 20% 6.3V X5R 805
C7841 22uF 20% 6.3V X5R 805
C7842 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C7843 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF

Vout = 0.6V * (1 + Ra / Rb)

1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	78	103

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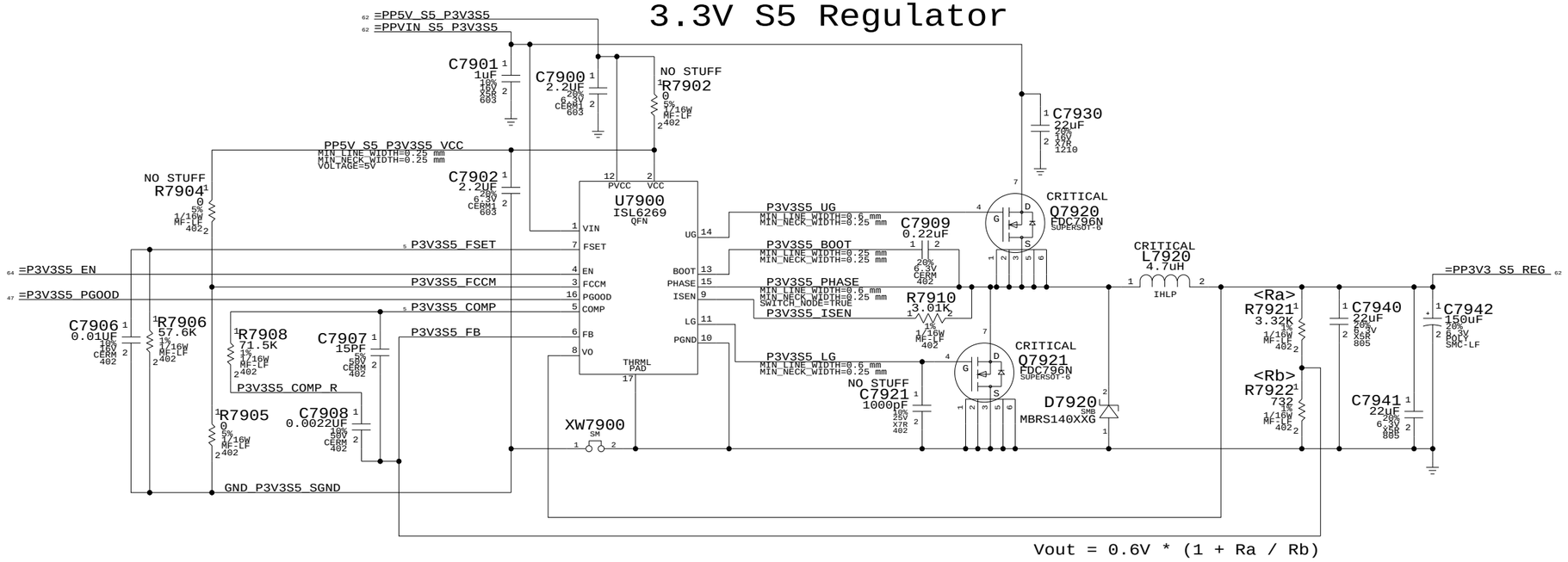
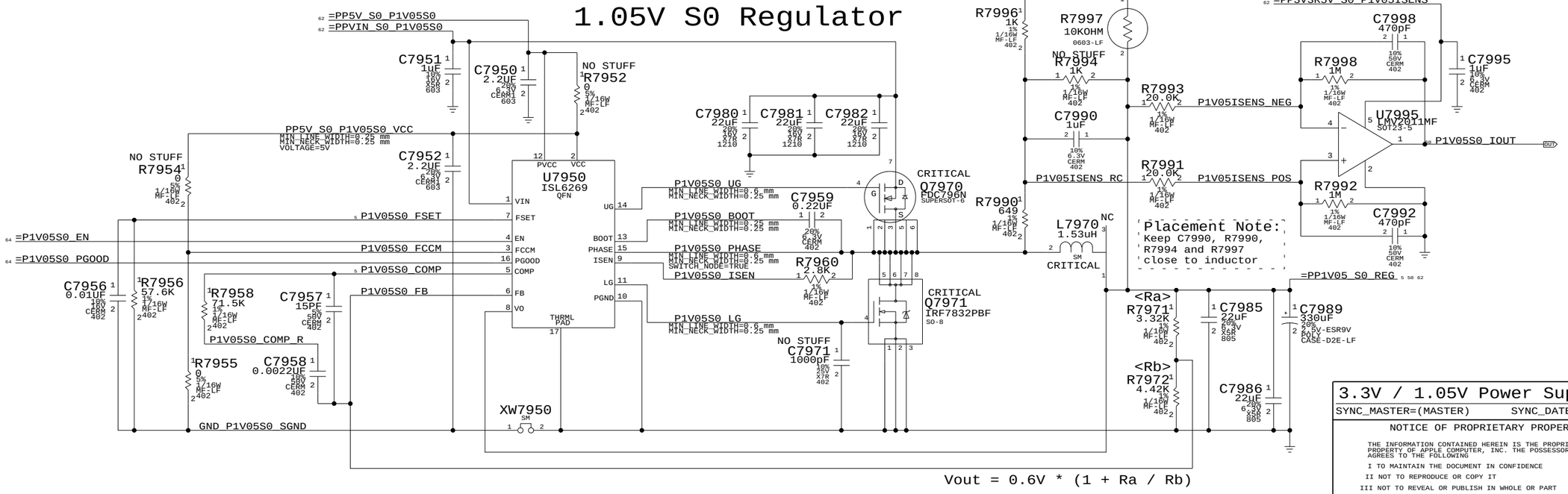
3.3V S5 Regulator



1.05V S0 Regulator



1.05V Current Sense

3.3V / 1.05V Power Supplies

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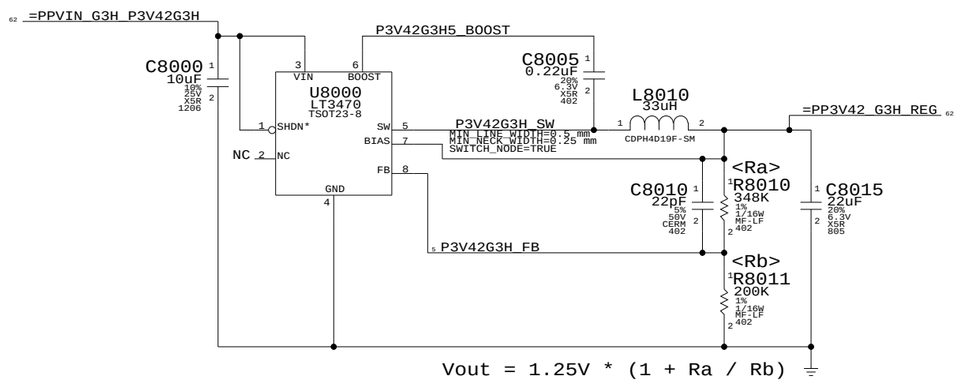
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

3.3V G3Hot Supply		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

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	SCALE: NONE	SHT: 80 OF 103	

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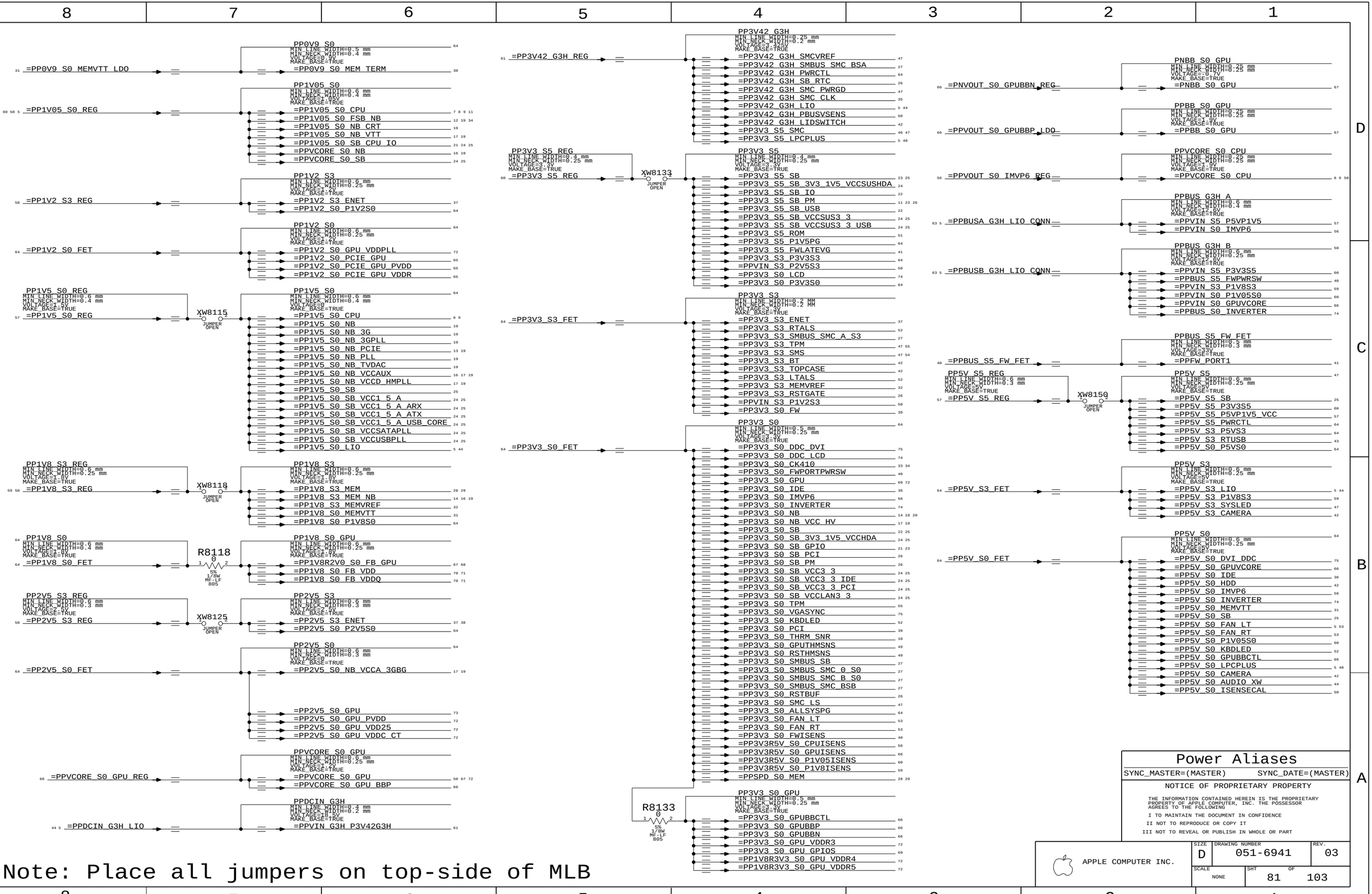

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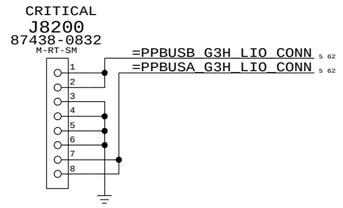
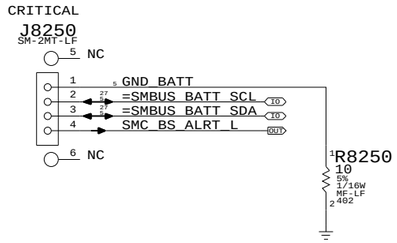
Left I/O Power Connector



Battery Connector (Digital Signals)



PBus-In & Battery Connectors

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D	051-6941	03

SCALE: NONE

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Unused PGOOD Signals

=P5VP1V5_PGOOD (57) — TP_P5V_P1V5_PGOOD — MAKE_BASE=TRUE
=P2V5S3_PGOOD (58) — TP_P2V5S3_PGOOD — MAKE_BASE=TRUE
=P1V8S3_PGOOD (59) — TP_P1V8S3_PGOOD — MAKE_BASE=TRUE
=P1V2S3_PGOOD (58) — TP_P1V2S3_PGOOD — MAKE_BASE=TRUE

These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Power Control Signals

=PP5V_S5_PWRCTL (64,62)

R8350 100K 5% 1/16W MF-LF 402
R8351 10K 5% 1/16W MF-LF 402

PM_SLP_S3_LS5V_L — MAKE_BASE=TRUE
Q8350 2N7002DW-X-F SOT-363
=P2V5S0_EN (64)
=P1V8S0_EN (64)
=P1V2S0_EN (64)

PM_SLP_S3_LS5V — MAKE_BASE=TRUE
Q8350 2N7002DW-X-F SOT-363
=P5VS0_EN_L (64)
=P3V3S0_EN_L (64)
LIO_P3V3S0_EN_L (5,44)
P1V5S0_RUNSS (5,57)

PM_SLP_S3_L (46,23) (TN)
R8356 100K 5% 1/16W MF-LF 402
1.5V Enable has pull-up to PBUS
Q8357 2N7002DW-X-F SOT-363

(PM_SLP_S3_L) — MAKE_BASE=TRUE
=P1V05S0_EN (60)
=GPUVCORE_EN (66)
=MEMVREF_EN (32)

=PP5V_S5_PWRCTL (64,62)
R8355 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V — MAKE_BASE=TRUE
Q8355 2N7002DW-X-F SOT-363
=P5VS3_EN_L (64)
=P3V3S3_EN_L (64)
P1V2S3_RUNSS (5,58)
1.2V Enable has pull-up to 3.3V
Q8355 2N7002DW-X-F SOT-363

PM_SLP_S4_L (46,23) (TN)
R8357 100K 5% 1/16W MF-LF 402

(PM_SLP_S4_L) — MAKE_BASE=TRUE
=P1V8S3_EN (59)
=RTUSB_EN (43)
LIO_P3V3S3_EN (5,44)
Q8358 TP0610 SOT23-3
PPVIN_S3_P2V5S3 (58)
P2V5S3_SHDNRT (5,58)
2.5V SHDN/RT pin has dual purpose and pull-down at regulator.

=PP3V42_G3H_PWRCTL (62)
SMC_PM_G2_EN (50,46) (TN)
R8358 100K 5% 1/16W MF-LF 402

(SMC_PM_G2_EN) — MAKE_BASE=TRUE
=P3V3S5_EN (60)
R8359 470K 5% 1/16W MF-LF 402
P5VS5_RUNSS (5,57)
5V Enable has pull-up to PBUS
SMC_PM_G2_EN_L
Q8359 2N7002DW-X-F SOT-363
Q8359 2N7002DW-X-F SOT-363

5V S3 FET

=PP5V_S3_P5VS3 (62) → Q8300 FDC638P SM-LF → =PP5V_S3_FET (62)
=P5VS3_EN_L (64) → R8300 0 5% 1/16W MF-LF 402 → P5VS3_EN_L_RC
C8300 0.0022uF 10% 50V CERM 402

5V S0 FET

=PP5V_S0_P5VS0 (62) → Q8305 FDC638P SM-LF → =PP5V_S0_FET (62)
=P5VS0_EN_L (64) → R8305 0 5% 1/16W MF-LF 402 → P5VS0_EN_L_RC
C8305 0.0022uF 10% 50V CERM 402
C8307 22uF 20% 6.3V X5R 805
C8306 22uF 20% 6.3V X5R 805

2.5V S0 FET

=PP2V5_S0_P2V5S0 (62) → Q8320 SI3446DV TSOP-LF → =PP2V5_S0_FET (62)
C8320 0.0022uF 10% 50V CERM 402
=P2V5S0_EN (64) → R8320 0 5% 1/16W MF-LF 402 → P2V5S0_EN_RC

3.3V S3 FET

=PP3V3_S3_P3V3S3 (62) → Q8310 FDC638P SM-LF → =PP3V3_S3_FET (62)
=P3V3S3_EN_L (64) → R8310 0 5% 1/16W MF-LF 402 → P3V3S3_EN_L_RC
C8310 0.0022uF 10% 50V CERM 402

3.3V S0 FET

=PP3V3_S0_P3V3S0 (62) → Q8315 FDC638P SM-LF → =PP3V3_S0_FET (62)
=P3V3S0_EN_L (64) → R8315 0 5% 1/16W MF-LF 402 → P3V3S0_EN_L_RC
C8315 0.0022uF 10% 50V CERM 402

1.8V S0 FET

=PP1V8_S0_P1V8S0 (62) → Q8325 FDC796N SUPERSOT-6 → =PP1V8_S0_FET (62)
C8325 0.0022uF 10% 50V CERM 402
=P1V8S0_EN (64) → R8325 0 5% 1/16W MF-LF 402 → P1V8S0_EN_RC
C8326 22uF 20% 6.3V X5R 805
C8327 22uF 20% 6.3V X5R 805

1.2V S0 FET

=PP1V2_S0_P1V2S0 (62) → Q8330 SI3446DV TSOP-LF → =PP1V2_S0_FET (62)
C8330 0.0022uF 10% 50V CERM 402
=P1V2S0_EN (64) → R8330 0 5% 1/16W MF-LF 402 → P1V2S0_EN_RC

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S5_P1V5PG (62)
PP1V5_S0 (62)
R8361 27.4K 1% 1/16W MF-LF 402
R8363 4.99K 1% 1/16W MF-LF 402
C8360 0.1uF 20% 10V CERM 402
0.89V Reference
P1V0_P1V5PG_REF
U8360 LMC7211 SM-LF (V+, V-)
P1V5S0_PGOOD
P1V5S0_COMP_POS
R8362 10K 1% 1/16W MF-LF 402
R8364 10K 1% 1/16W MF-LF 402
R8365 10K 5% 1/16W MF-LF 402
1.5V Comp threshold set to 1.32V (88%)
IMVP_PWRGD_IN (56) (OUT)

=P1V05S0_PGOOD (60) (TN)
ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8365 acts as 10K pull-up for PGOOD signal
P1V5P1V05S0_PGOOD — MAKE_BASE=TRUE

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0 (62)
PP3V3_S0 (62)
PP2V5_S0 (62)
PP1V8_S0 (62)
PP1V2_S0 (62)
PP0V9_S0 (62)

R8374 68.1K 1% 1/16W MF-LF 402
R8372 124K 1% 1/16W MF-LF 402
R8375 100K 1% 1/16W MF-LF 402
R8373 100K 1% 1/16W MF-LF 402
S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV
C8370 0.1uF 20% 10V CERM 402
C8371 0.1uF 20% 10V CERM 402
U8370 LTC2908 LLP (V1, V2, V3, V4 CRITICAL, VADJ1, VADJ2, RST*, GND, THRML PAD)
S0PGOOD_PWROK
R8376 549K 1% 1/16W MF-LF 402
LTC2908 sources 6uA at 5.0V
R8375 serves as pull-down
and 3.3V level-shifter.
LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

=PP3V3_S0_ALLSYSPG (62)
U8380 MC74VHC1G08 SC70 — ALL_SYS_PWRGD (OUT)
C8380 0.1UF 20% 10V CERM 402

S3/S0 FETs & Power Control

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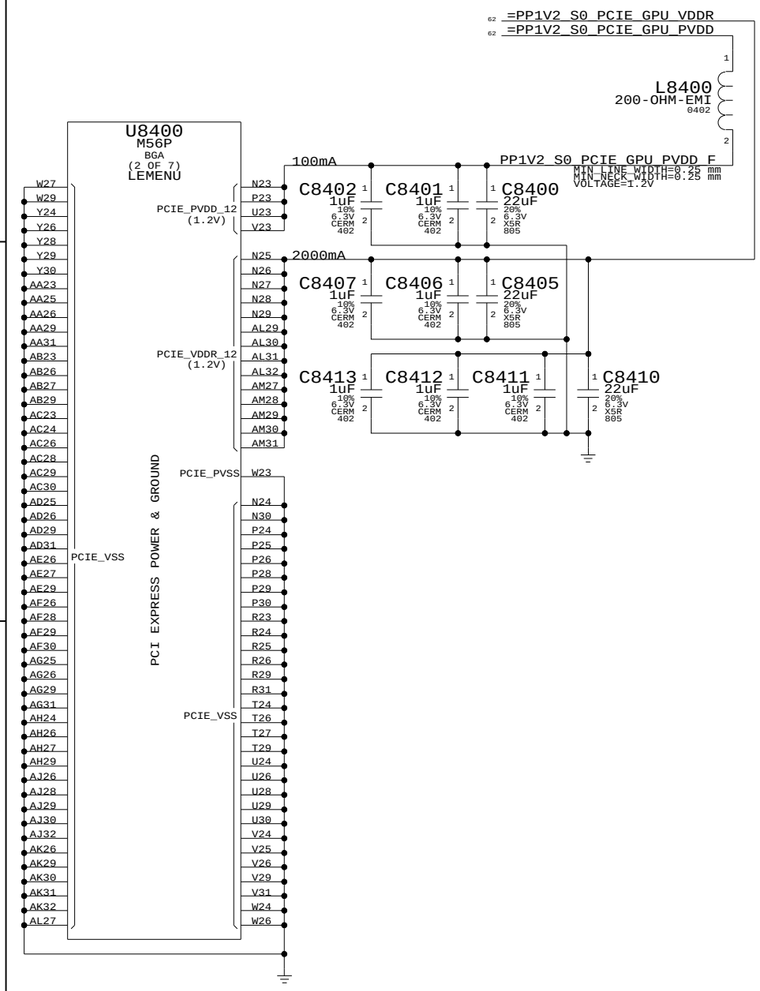
=PP1V2_S0_PCIE_GPU_VDDR 62
=PP1V2_S0_PCIE_GPU_PVDD 62
L8400
200-OHM-EMI
0402
U8400
M56P
BGA
(2 OF 7)
LEMENU
100mA
PP1V2_S0_PCIE_GPU_PVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
PCIE_PVDD_12
(1.2V)
C8402 1uF 10% 6.3V CERM 402
C8401 1uF 10% 6.3V CERM 402
C8400 22uF 20% 6.3V X5R 805
2000mA
C8407 1uF 10% 6.3V CERM 402
C8406 1uF 10% 6.3V CERM 402
C8405 22uF 20% 6.3V X5R 805
PCIE_VDDR_12
(1.2V)
C8413 1uF 10% 6.3V CERM 402
C8412 1uF 10% 6.3V CERM 402
C8411 1uF 10% 6.3V CERM 402
C8410 22uF 20% 6.3V X5R 805
PCIE_PVSS
PCIE_VSS
PCIE_VSS
PCI EXPRESS POWER & GROUND
N23 P23 U23 V23 N25 N26 N27 N28 N29 AL29 AL30 AL31 AL32 AM27 AM28 AM29 AM30 AM31 W23 N24 N30 P24 P25 P26 P28 P29 P30 R23 R24 R25 R26 R29 R31 T24 T26 T27 T29 U24 U26 U28 U29 U30 V24 V25 V26 V29 V31 W24 W26
W27 W29 Y24 Y26 Y28 Y29 Y30 AA23 AA25 AA26 AA29 AA31 AB23 AB26 AB27 AB29 AC23 AC24 AC26 AC28 AC29 AC30 AD25 AD26 AD29 AD31 AE26 AE27 AE29 AE26 AE28 AF29 AF30 AG25 AG26 AG29 AG31 AH24 AH26 AH27 AH29 AJ26 AJ28 AJ29 AJ30 AJ32 AK26 AK29 AK30 AK31 AK32 AL27
PCIE_VSS
LEMENU
U8400
M56P
BGA
(1 OF 7)
PCI-EXPRESS BUS INTERFACE
PEG_R2D_C_P<0> C8420 0.1uF PEG_R2D_P<0> AJ31 PCIE_RX0P
PEG_R2D_C_N<0> C8421 0.1uF PEG_R2D_N<0> AH31 PCIE_RX0N
PEG_R2D_C_P<1> C8422 0.1uF PEG_R2D_P<1> AH30 PCIE_RX1P
PEG_R2D_C_N<1> C8423 0.1uF PEG_R2D_N<1> AG30 PCIE_RX1N
PEG_R2D_C_P<2> C8424 0.1uF PEG_R2D_P<2> AG32 PCIE_RX2P
PEG_R2D_C_N<2> C8425 0.1uF PEG_R2D_N<2> AF32 PCIE_RX2N
PEG_R2D_C_P<3> C8426 0.1uF PEG_R2D_P<3> AF31 PCIE_RX3P
PEG_R2D_C_N<3> C8427 0.1uF PEG_R2D_N<3> AE31 PCIE_RX3N
PEG_R2D_C_P<4> C8428 0.1uF PEG_R2D_P<4> AE30 PCIE_RX4P
PEG_R2D_C_N<4> C8429 0.1uF PEG_R2D_N<4> AD30 PCIE_RX4N
PEG_R2D_C_P<5> C8430 0.1uF PEG_R2D_P<5> AD32 PCIE_RX5P
PEG_R2D_C_N<5> C8431 0.1uF PEG_R2D_N<5> AC32 PCIE_RX5N
PEG_R2D_C_P<6> C8432 0.1uF PEG_R2D_P<6> AC31 PCIE_RX6P
PEG_R2D_C_N<6> C8433 0.1uF PEG_R2D_N<6> AB31 PCIE_RX6N
PEG_R2D_C_P<7> C8434 0.1uF PEG_R2D_P<7> AB30 PCIE_RX7P
PEG_R2D_C_N<7> C8435 0.1uF PEG_R2D_N<7> AA30 PCIE_RX7N
PEG_R2D_C_P<8> C8436 0.1uF PEG_R2D_P<8> AA32 PCIE_RX8P
PEG_R2D_C_N<8> C8437 0.1uF PEG_R2D_N<8> Y32 PCIE_RX8N
PEG_R2D_C_P<9> C8438 0.1uF PEG_R2D_P<9> Y31 PCIE_RX9P
PEG_R2D_C_N<9> C8439 0.1uF PEG_R2D_N<9> W31 PCIE_RX9N
PEG_R2D_C_P<10> C8440 0.1uF PEG_R2D_P<10> W30 PCIE_RX10P
PEG_R2D_C_N<10> C8441 0.1uF PEG_R2D_N<10> V30 PCIE_RX10N
PEG_R2D_C_P<11> C8442 0.1uF PEG_R2D_P<11> V32 PCIE_RX11P
PEG_R2D_C_N<11> C8443 0.1uF PEG_R2D_N<11> U32 PCIE_RX11N
PEG_R2D_C_P<12> C8444 0.1uF PEG_R2D_P<12> U31 PCIE_RX12P
PEG_R2D_C_N<12> C8445 0.1uF PEG_R2D_N<12> T31 PCIE_RX12N
PEG_R2D_C_P<13> C8446 0.1uF PEG_R2D_P<13> T30 PCIE_RX13P
PEG_R2D_C_N<13> C8447 0.1uF PEG_R2D_N<13> R30 PCIE_RX13N
PEG_R2D_C_P<14> C8448 0.1uF PEG_R2D_P<14> R32 PCIE_RX14P
PEG_R2D_C_N<14> C8449 0.1uF PEG_R2D_N<14> P32 PCIE_RX14N
PEG_R2D_C_P<15> C8450 0.1uF PEG_R2D_P<15> P31 PCIE_RX15P
PEG_R2D_C_N<15> C8451 0.1uF PEG_R2D_N<15> N31 PCIE_RX15N
PEG_CLK100M_GPU_P AL28 PCIE_REFCLKP
PEG_CLK100M_GPU_N AK28 PCIE_REFCLKN
PEG_RESET_L AG24 PERST*
AF24 PERST*_MASK
NC AA24 PCIE_TEST
PCIE_TX0P AK27 PEG_D2R_C_P<0> C8455 0.1uF PEG_D2R_P<0> OUT
PCIE_TX0N AJ27 PEG_D2R_C_N<0> C8456 0.1uF PEG_D2R_N<0> OUT
PCIE_TX1P AJ25 PEG_D2R_C_P<1> C8457 0.1uF PEG_D2R_P<1> OUT
PCIE_TX1N AH25 PEG_D2R_C_N<1> C8458 0.1uF PEG_D2R_N<1> OUT
PCIE_TX2P AH28 PEG_D2R_C_P<2> C8459 0.1uF PEG_D2R_P<2> OUT
PCIE_TX2N AG28 PEG_D2R_C_N<2> C8460 0.1uF PEG_D2R_N<2> OUT
PCIE_TX3P AG27 PEG_D2R_C_P<3> C8461 0.1uF PEG_D2R_P<3> OUT
PCIE_TX3N AF27 PEG_D2R_C_N<3> C8462 0.1uF PEG_D2R_N<3> OUT
PCIE_TX4P AF25 PEG_D2R_C_P<4> C8463 0.1uF PEG_D2R_P<4> OUT
PCIE_TX4N AE25 PEG_D2R_C_N<4> C8464 0.1uF PEG_D2R_N<4> OUT
PCIE_TX5P AE28 PEG_D2R_C_P<5> C8465 0.1uF PEG_D2R_P<5> OUT
PCIE_TX5N AD28 PEG_D2R_C_N<5> C8466 0.1uF PEG_D2R_N<5> OUT
PCIE_TX6P AD27 PEG_D2R_C_P<6> C8467 0.1uF PEG_D2R_P<6> OUT
PCIE_TX6N AC27 PEG_D2R_C_N<6> C8468 0.1uF PEG_D2R_N<6> OUT
PCIE_TX7P AC25 PEG_D2R_C_P<7> C8469 0.1uF PEG_D2R_P<7> OUT
PCIE_TX7N AB25 PEG_D2R_C_N<7> C8470 0.1uF PEG_D2R_N<7> OUT
PCIE_TX8P AB28 PEG_D2R_C_P<8> C8471 0.1uF PEG_D2R_P<8> OUT
PCIE_TX8N AA28 PEG_D2R_C_N<8> C8472 0.1uF PEG_D2R_N<8> OUT
PCIE_TX9P AA27 PEG_D2R_C_P<9> C8473 0.1uF PEG_D2R_P<9> OUT
PCIE_TX9N Y27 PEG_D2R_C_N<9> C8474 0.1uF PEG_D2R_N<9> OUT
PCIE_TX10P Y25 PEG_D2R_C_P<10> C8475 0.1uF PEG_D2R_P<10> OUT
PCIE_TX10N W25 PEG_D2R_C_N<10> C8476 0.1uF PEG_D2R_N<10> OUT
PCIE_TX11P W28 PEG_D2R_C_P<11> C8477 0.1uF PEG_D2R_P<11> OUT
PCIE_TX11N V28 PEG_D2R_C_N<11> C8478 0.1uF PEG_D2R_N<11> OUT
PCIE_TX12P V27 PEG_D2R_C_P<12> C8479 0.1uF PEG_D2R_P<12> OUT
PCIE_TX12N U27 PEG_D2R_C_N<12> C8480 0.1uF PEG_D2R_N<12> OUT
PCIE_TX13P U25 PEG_D2R_C_P<13> C8481 0.1uF PEG_D2R_P<13> OUT
PCIE_TX13N T25 PEG_D2R_C_N<13> C8482 0.1uF PEG_D2R_N<13> OUT
PCIE_TX14P T28 PEG_D2R_C_P<14> C8483 0.1uF PEG_D2R_P<14> OUT
PCIE_TX14N R28 PEG_D2R_C_N<14> C8484 0.1uF PEG_D2R_N<14> OUT
PCIE_TX15P R27 PEG_D2R_C_P<15> C8485 0.1uF PEG_D2R_P<15> OUT
PCIE_TX15N P27 PEG_D2R_C_N<15> C8486 0.1uF PEG_D2R_N<15> OUT
10% 16V X5R 402
=PP1V2_S0_PCIE_GPU 62
R8495 2.0K 1% 1/16W MF-LF 402
PCIE_CALRP AD24 GPU_PCIE_CALRP
PCIE_CALRN AE24 GPU_PCIE_CALRN
PCIE_CALI AB24 GPU_PCIE_CALI
R8497 1.47K 1% 1/16W MF-LF 402
R8496 562 1% 1/16W MF-LF 402

ATI M56 PCI-E

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D	051-6941	03
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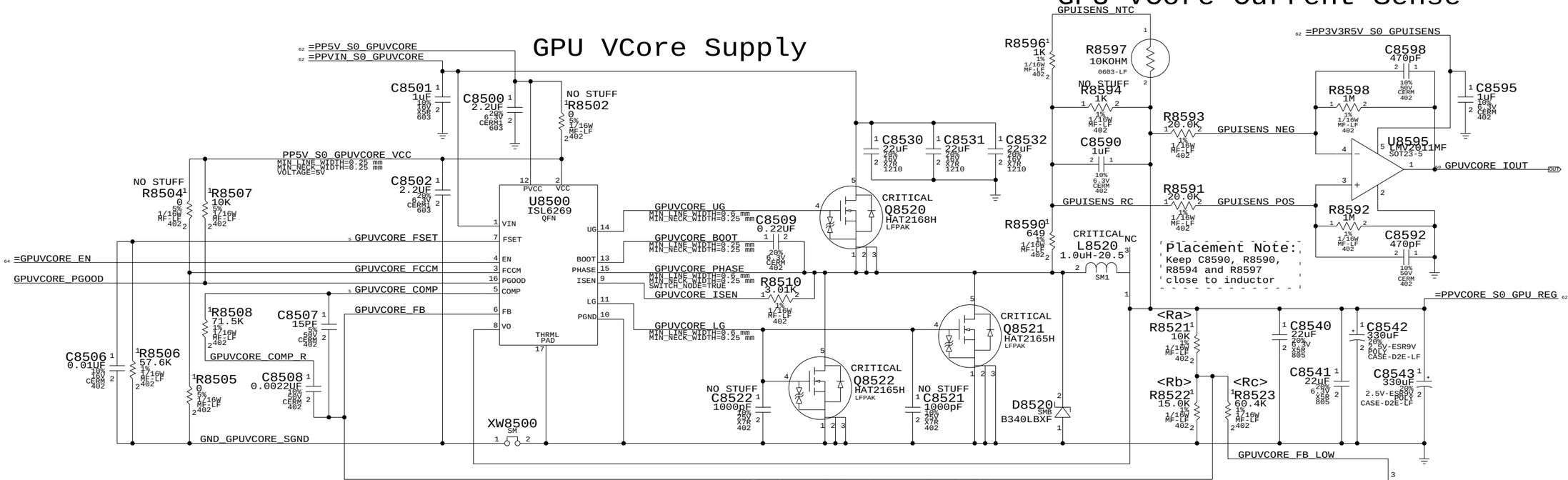
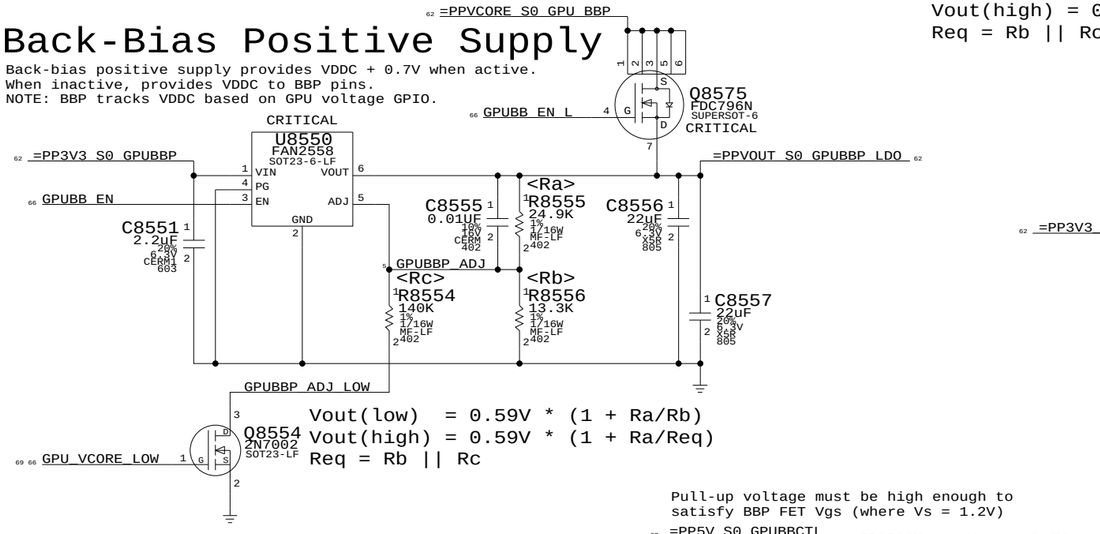
GPU VCore Supply



Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

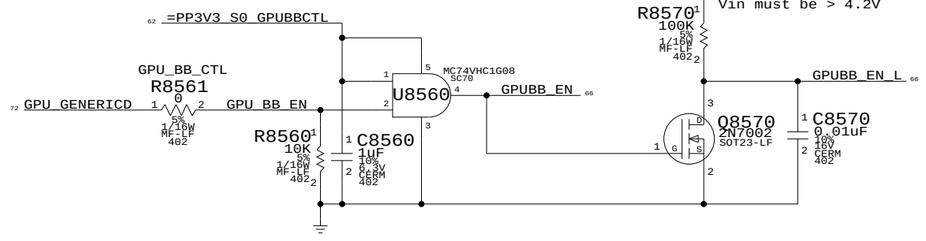
Back-bias positive supply provides VDDC + 0.7V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

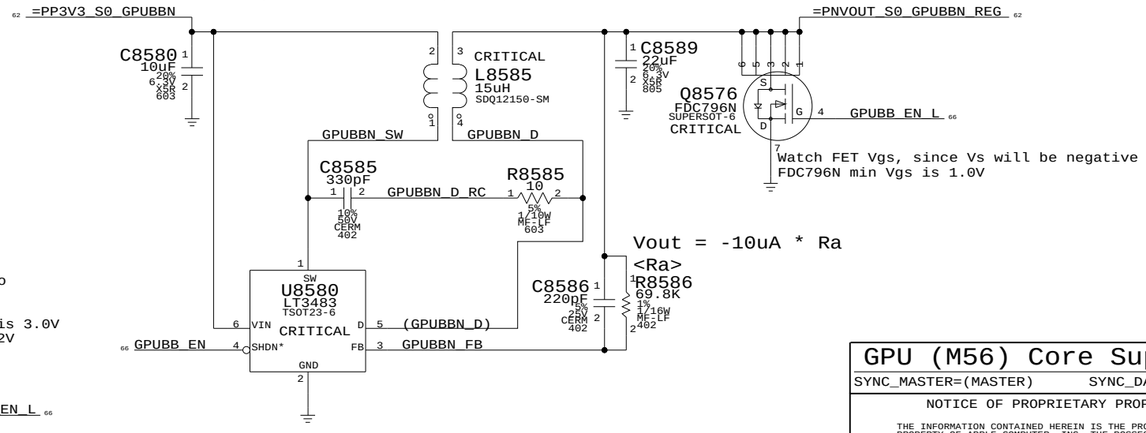
Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

FDC796N max Vgs is 3.0V
Vin must be > 4.2V



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.7V when active.
When inactive, provides VSS to BBN pins.



Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V

Vout = -10uA * Ra

GPU VCore Current Sense

GPU (M56) Core Supplies

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D	051-6941	03
SCALE: NONE	SHT 85 OF 103	

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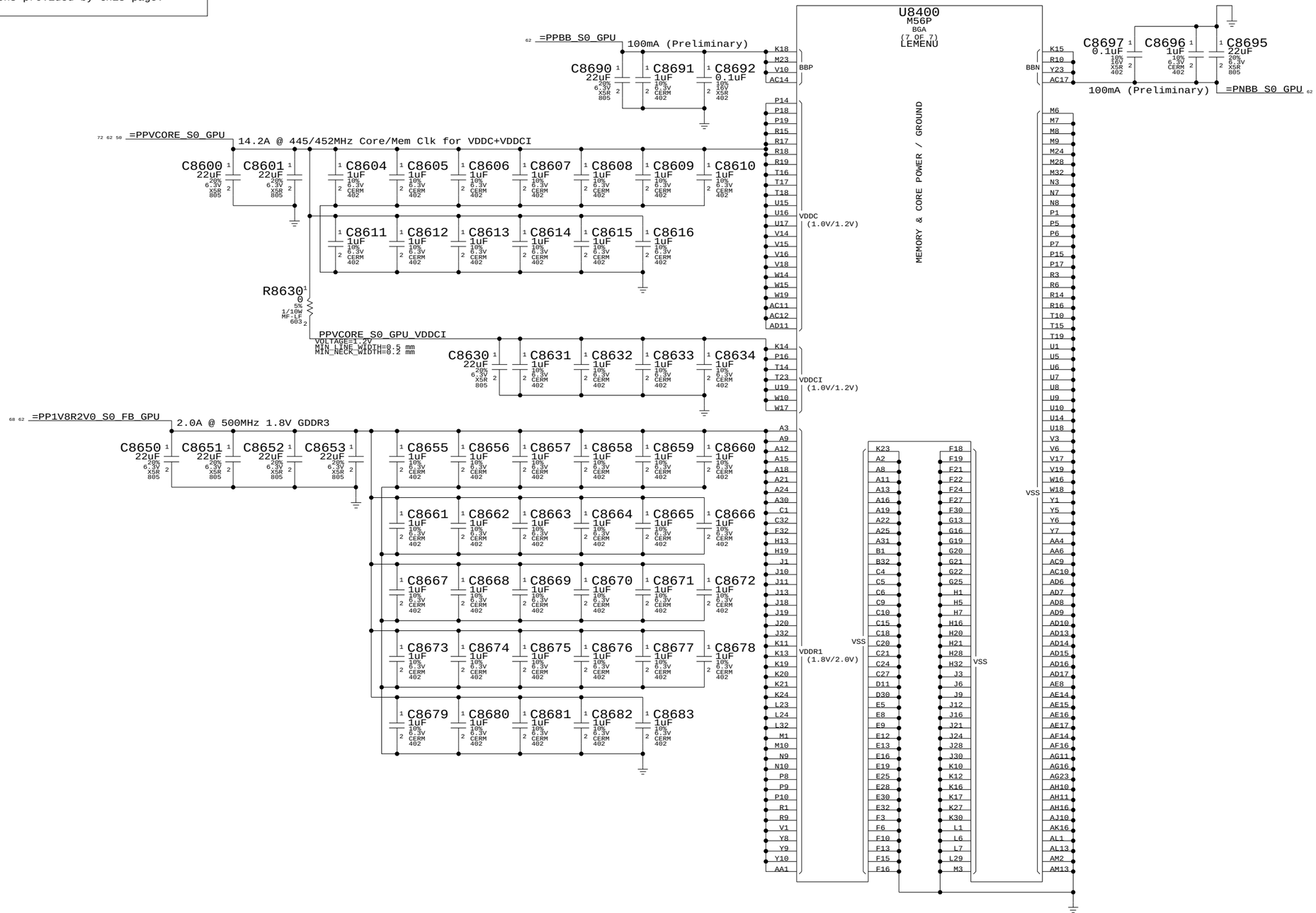
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	86	103

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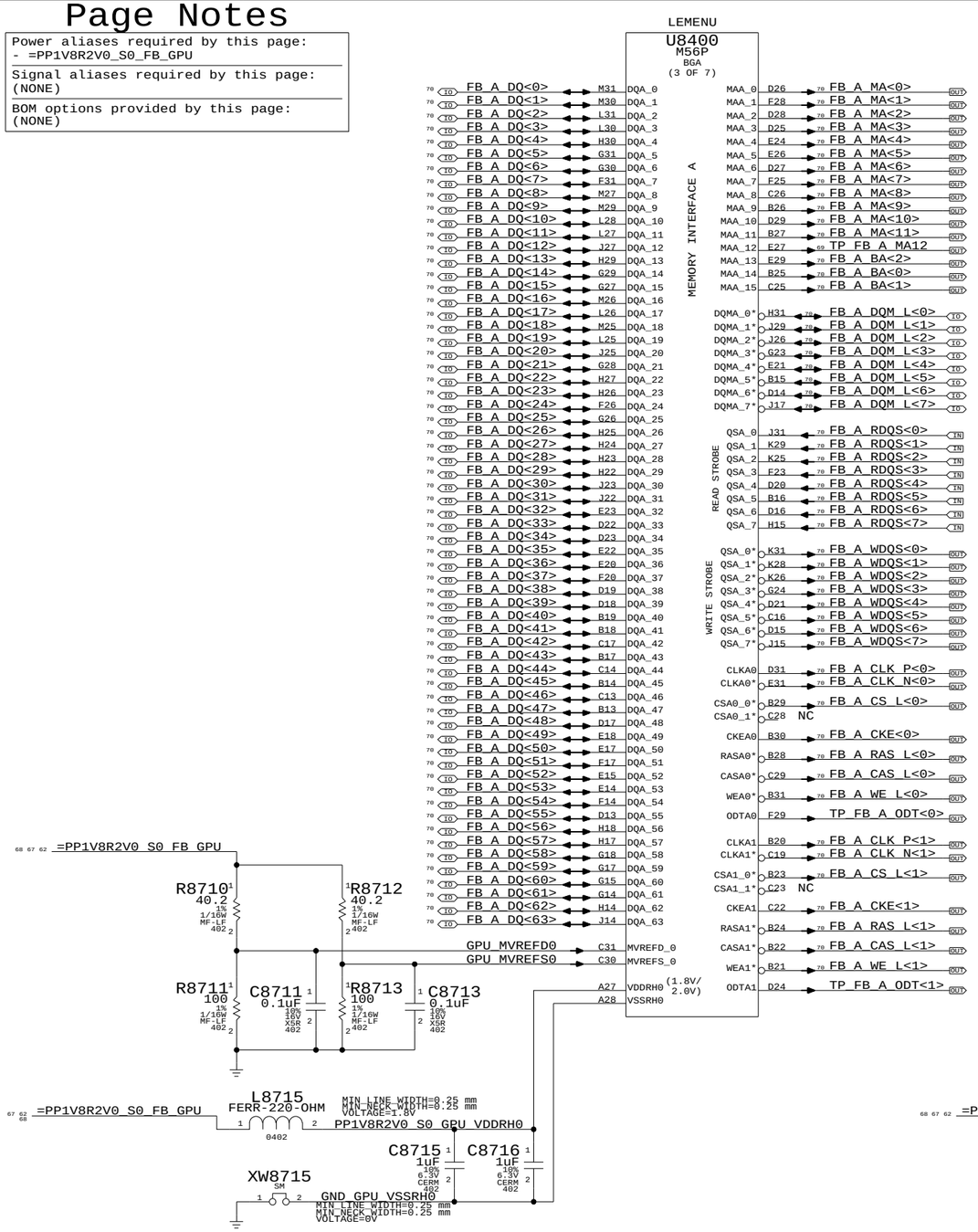
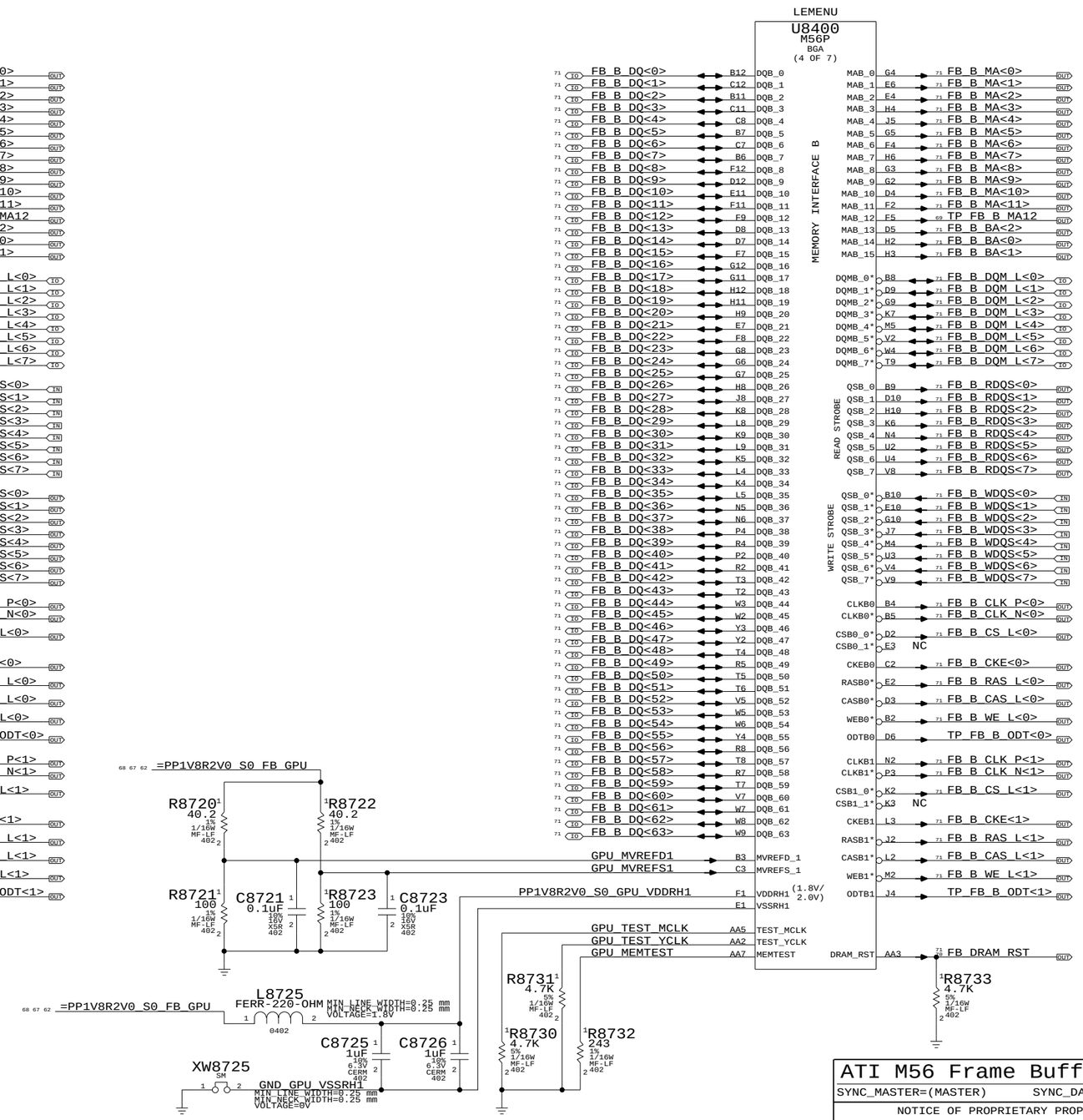
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	87	103

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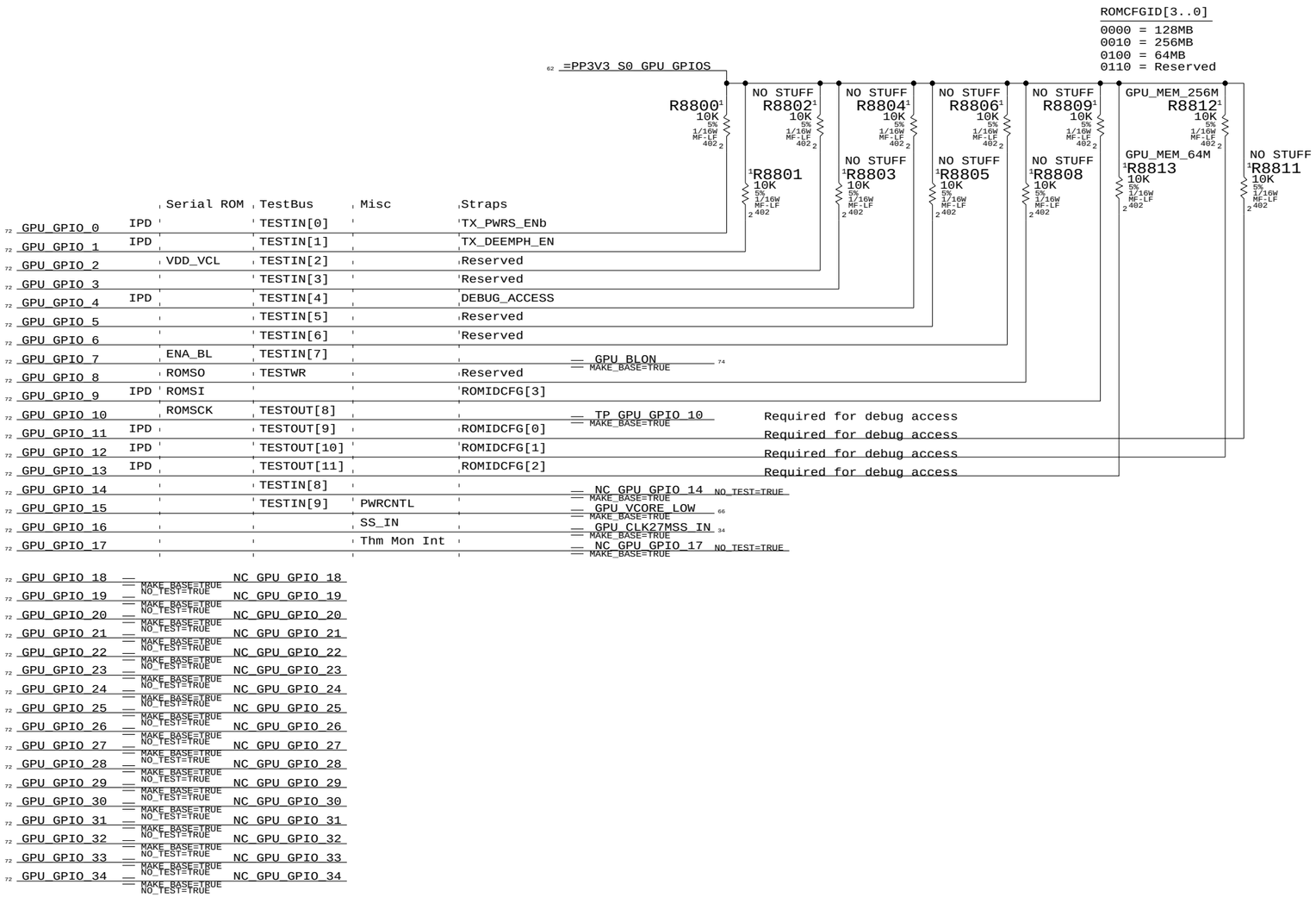


Renamed signals

GPU_CLK27M (34) — GPU_XTALIN (72)

Unused signals

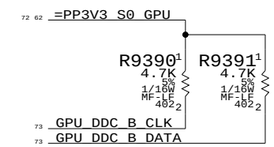
NC_GPU_XTALOUT — GPU_XTALOUT (72)
NC_ATI_ROMCS_L — TP_ATI_ROMCS_L (72)
NC_FB_A_MA12 — TP_FB_A_MA12 (68)
NC_FB_B_MA12 — TP_FB_B_MA12 (68)
NC_GPU_GENERICA — GPU_GENERICA (72)
NC_GPU_GENERICB — GPU_GENERICB (72)
NC_GPU_GENERICC — GPU_GENERICC (72)
NC_GPU_VGA_R — GPU_VGA_R (73)
NC_GPU_VGA_G — GPU_VGA_G (73)
NC_GPU_VGA_B — GPU_VGA_B (73)
NC_GPU_VGA_HSYNC — GPU_VGA_HSYNC (73)
NC_GPU_VGA_VSYNC — GPU_VGA_VSYNC (73)
NC_GPU_R2 — GPU_R2 (73)
NC_GPU_G2 — GPU_G2 (73)
NC_GPU_B2 — GPU_B2 (73)
NC_LVDS_U_DATAP<3> — LVDS_U_DATA_P<3> (73)
NC_LVDS_U_DATAN<3> — LVDS_U_DATA_N<3> (73)
NC_LVDS_L_DATAP<3> — LVDS_L_DATA_P<3> (73)
NC_LVDS_L_DATAN<3> — LVDS_L_DATA_N<3> (73)
NC_ATI_DVPCLK — ATI_DVPCLK (72)
NC_ATI_DVPCNTL<2..0> — ATI_DVPCNTL<2..0> (72)
NC_ATI_DVPDATA<15..0> — ATI_DVPDATA<15..0> (72)

(MAKE_BASE=TRUE, NO_TEST=TRUE)

Required for debug access

TP_ATI_DVPDATA<23..16> — ATI_DVPDATA<23..16> (72)

Also required: GPIO10 - GPIO13



GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	88	103

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

Connect to designated pin, then GND

Connect to designated pin, then GND

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03

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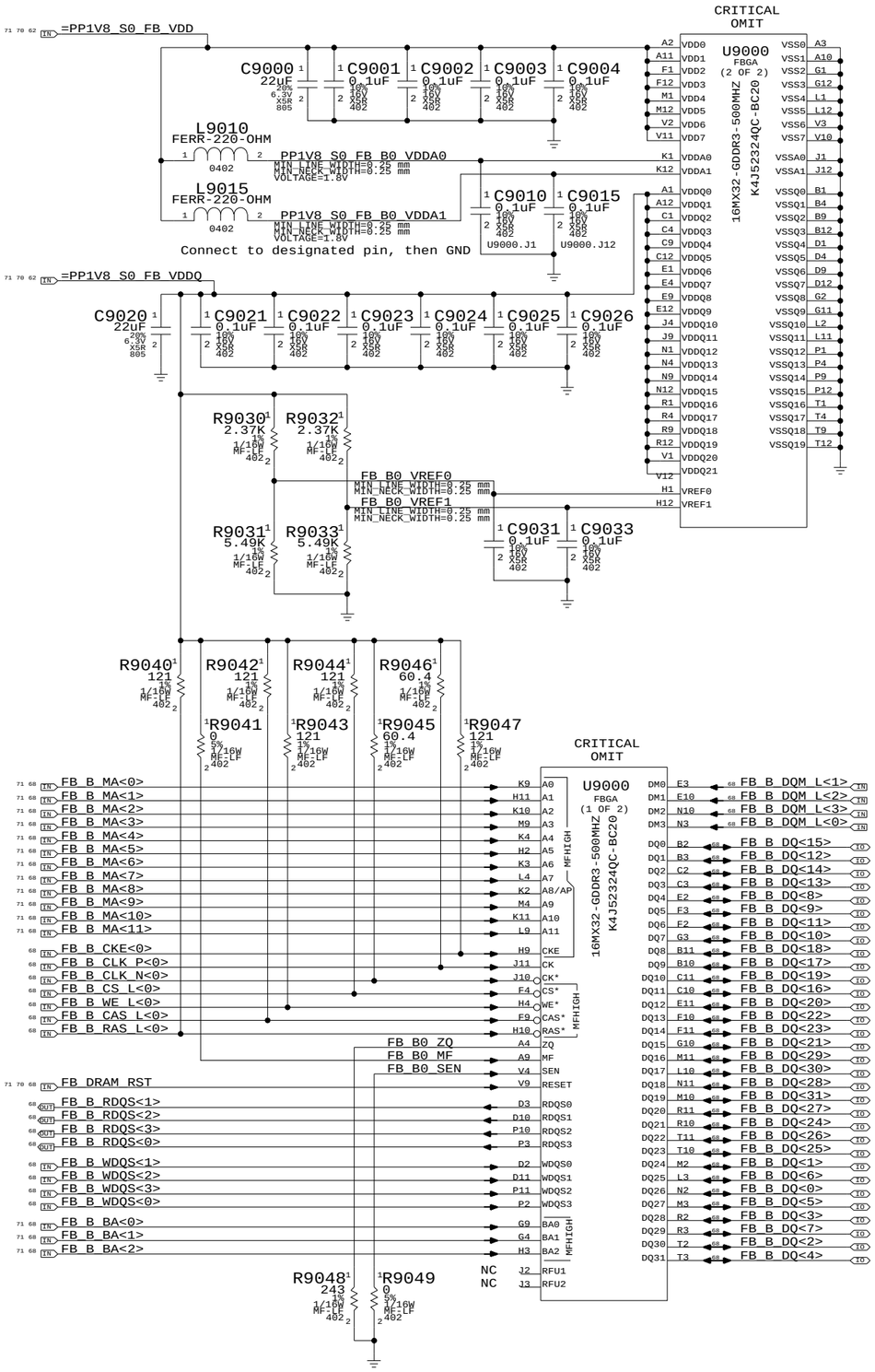
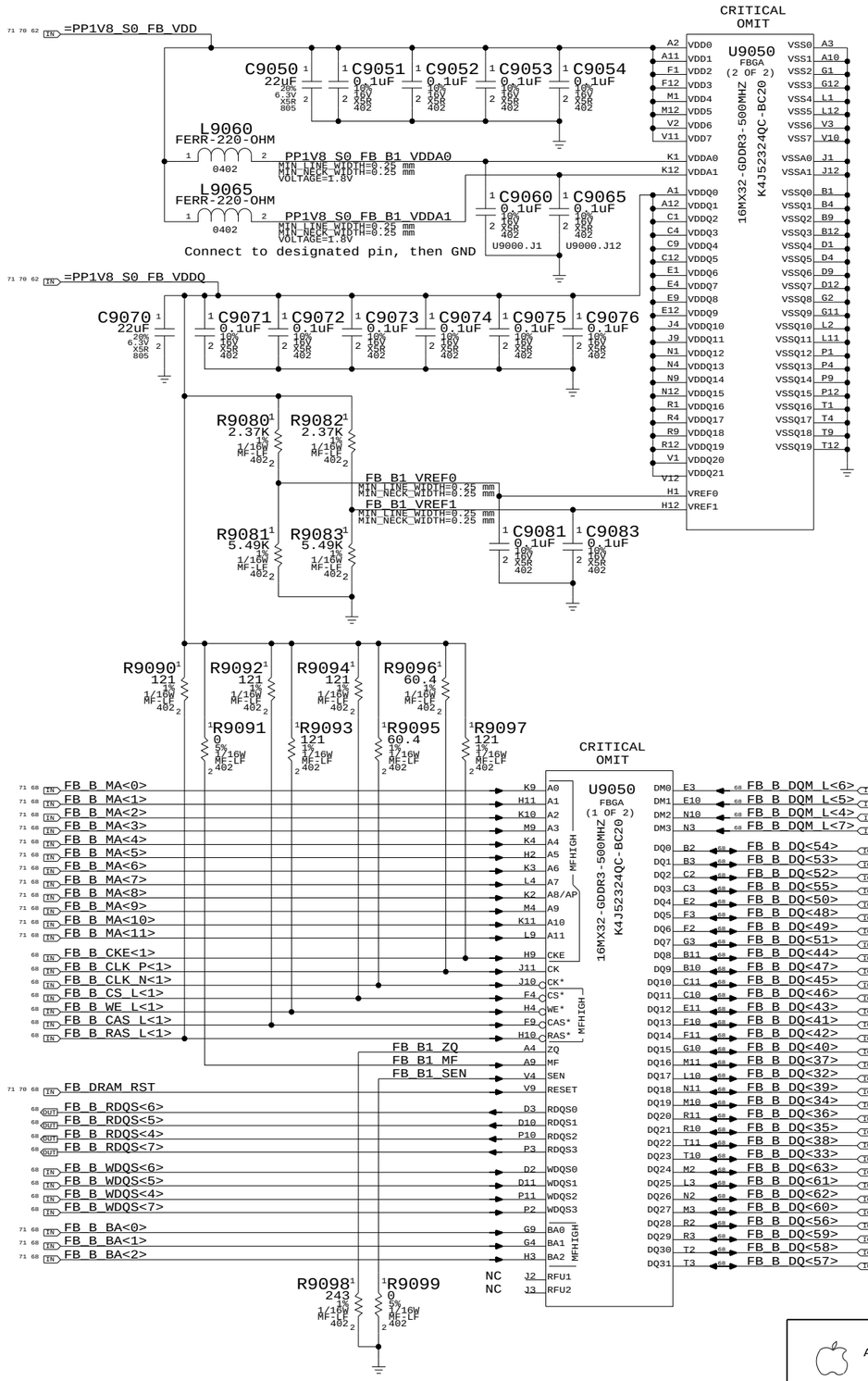
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	90	103

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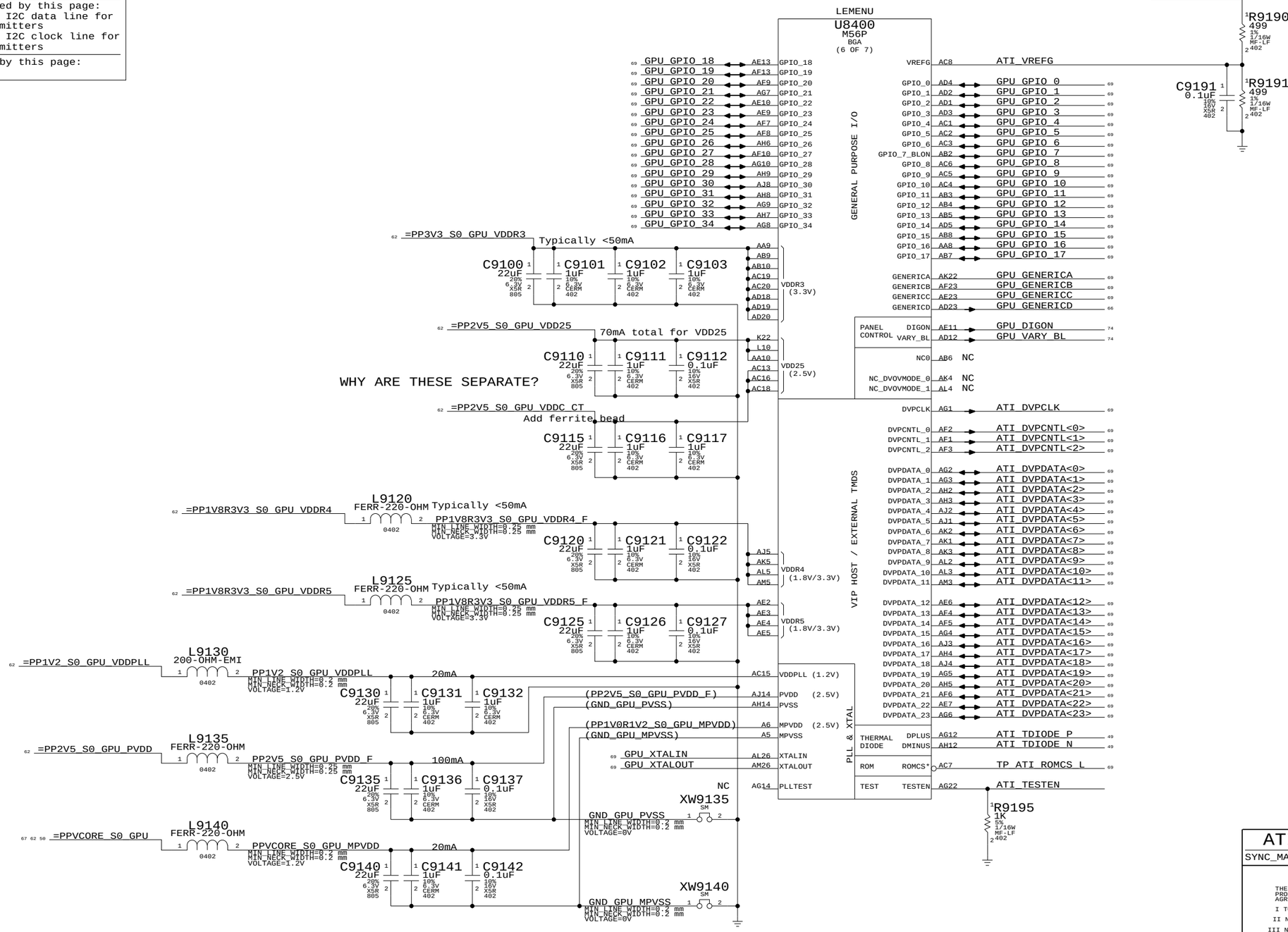
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

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NONE	91	103

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Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

62 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22uF 20% 6.3V X5R 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22uF 20% 6.3V X5R 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22uF 20% 6.3V X5R 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22uF 20% 6.3V X5R 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22uF 20% 6.3V X5R 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V — 20mA peak
C9325 22uF 20% 6.3V X5R 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22uF 20% 6.3V X5R 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22uF 20% 6.3V X5R 805; C9345 22uF 20% 6.3V X5R 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

ATI_RSET 73 — R9350 499 1% 1/16W MF-LF 402 — GND
ATI_R2SET 73 — R9351 715 1% 1/16W MF-LF 402 — GND

LEMENU
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS

AM8	TPVDD (2.5V)		
AL8	TPVSS		
AJ6	TXVDDR (2.5V)		
AK6			
AL6			
AM6			
AJ7	TXVSSR		
AK7			
AK8			
AL7			
AM7			
TXCP	AM9	76 75 74	TMDS_CLK_P
TXCM	AL9	76 75 74	TMDS_CLK_N
TX0P	AL10	76 75 74	TMDS_DATA_P<0>
TX0M	AK10	76 75 74	TMDS_DATA_N<0>
TX1P	AM11	76 75 74	TMDS_DATA_P<1>
TX1M	AL11	76 75 74	TMDS_DATA_N<1>
TX2P	AM12	76 75 74	TMDS_DATA_P<2>
TX2M	AL12	76 75 74	TMDS_DATA_N<2>
TX3P	AJ9	76 75 74	TMDS_DATA_P<3>
TX3M	AK9	76 75 74	TMDS_DATA_N<3>
TX4P	AJ11	76 75 74	TMDS_DATA_P<4>
TX4M	AK11	76 75 74	TMDS_DATA_N<4>
TX5P	AJ12	76 75 74	TMDS_DATA_P<5>
TX5M	AK12	76 75 74	TMDS_DATA_N<5>

DAC (CRT)

AL25	AVDD (2.5V)		
AM25			
AJ24	AVSS		
AK25			
AK23	AVSSQ		
AM23	VDD1DI (2.5V)		
AL23	VSS1DI		
AL22	RSET		
R	AK24	69	GPU_VGA_R
G	AM24	69	GPU_VGA_G
B	AL24	69	GPU_VGA_B
HSYNC	AJ23	69	GPU_VGA_HSYNC
VSYNC	AJ22	69	GPU_VGA_VSYNC

DAC2 (TV/CRT2)

AL16	A2VDD (2.5V)		
AM16			
AL17	A2VSS		
AM17			
NC	AL14 NC_A2VDDQ		
AK13	A2VSSQ		
AJ16	VDD2DI (2.5V)		
AJ17	VSS2DI		
AK14	R2SET		
R2	AK15	69	GPU_R2
G2	AM15	69	GPU_G2
B2	AL15	69	GPU_B2
H2SYNC	AE15	78	GPU_H2SYNC
V2SYNC	AG15	78	GPU_V2SYNC
Y	AJ15	78 74	GPU_TV_Y
C	AJ13	78 74	GPU_TV_C
COMP	AH15	78 74	GPU_TV_COMP

LVDS

AE19	LVPDD (2.5V)		
AE18	LVPSS		
AC21	LVDDR (2.5V)		
AC22			
AD21			
AD22			
AE20			
AE21			
AE22			
AF19			
AF20			
AF17	LVSSR		
AF18			
AF21			
AF22			
AG17			
AG19			
AH17			
AH19			
AJ19			
AK17			
TXCLK_UP	AJ21	74	LVDS_U_CLK_P
TXCLK_UN	AK21	74	LVDS_U_CLK_N
TXOUT_U0P	AG18	74	LVDS_U_DATA_P<0>
TXOUT_U0N	AH18	74	LVDS_U_DATA_N<0>
TXOUT_U1P	AK20	74	LVDS_U_DATA_P<1>
TXOUT_U1N	AJ20	74	LVDS_U_DATA_N<1>
TXOUT_U2P	AG20	74	LVDS_U_DATA_P<2>
TXOUT_U2N	AH20	74	LVDS_U_DATA_N<2>
TXOUT_U3P	AH21	69	LVDS_U_DATA_P<3>
TXOUT_U3N	AG21	69	LVDS_U_DATA_N<3>
TXCLK_LP	AM18	74	LVDS_L_CLK_P
TXCLK_LN	AL18	74	LVDS_L_CLK_N
TXOUT_L0P	AL19	74	LVDS_L_DATA_P<0>
TXOUT_L0N	AK19	74	LVDS_L_DATA_N<0>
TXOUT_L1P	AM20	74	LVDS_L_DATA_P<1>
TXOUT_L1N	AL20	74	LVDS_L_DATA_N<1>
TXOUT_L2P	AM21	74	LVDS_L_DATA_P<2>
TXOUT_L2N	AL21	74	LVDS_L_DATA_N<2>
TXOUT_L3P	AJ18	69	LVDS_L_DATA_P<3>
TXOUT_L3N	AK18	69	LVDS_L_DATA_N<3>

MONITOR IDENTIFICATION

DDC1CLK	AH23	75	GPU_DDC_A_CLK
DDC1DATA	AH22	75	GPU_DDC_A_DATA
DDC2CLK	AG13	69	GPU_DDC_B_CLK
DDC2DATA	AH13	69	GPU_DDC_B_DATA
DDC3CLK	AF12	74	GPU_DDC_C_CLK
DDC3DATA	AE12	74	GPU_DDC_C_DATA
75 INT	GPU_HPD	AF11	HPD1

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_TV_Y
	VGA	VGA	GPU_TV_C
	VGA	VGA	GPU_TV_COMP
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

62 =PP3V3_S0_LCD

R9400 100K 5% 1/16W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

LCD_PWREN_L

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD2

LCD_CTL_SMC
R9494 0 5% 1/16W MF-LF 402

46 SMC_DISPLAY_ENABLE

GPU_OR_SMC_DISP_EN

Q9401 2N7002 SOT23-LF

LCD_CTL_GPU
R9495 0 5% 1/16W MF-LF 402

72 GPU_DIGON

62 =PP3V3_S0_DDC_LCD

100K pull-ups are for
no-panel case (development)
Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

73 GPU_DDC_C_CLK

73 GPU_DDC_C_DATA

C9410 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD3

6 =GND_CHASSIS_LCD1

C9420 0.001uF 20% 50V CERM 402

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

74 73 LVDS_L_DATA_N<0>
74 73 LVDS_L_DATA_P<0>
74 73 LVDS_L_DATA_N<1>
74 73 LVDS_L_DATA_P<1>
74 73 LVDS_L_DATA_N<2>
74 73 LVDS_L_DATA_P<2>
74 73 LVDS_L_CLK_N
74 73 LVDS_L_CLK_P
74 73 LVDS_U_DATA_N<0>
74 73 LVDS_U_DATA_P<0>
74 73 LVDS_U_DATA_N<1>
74 73 LVDS_U_DATA_P<1>
74 73 LVDS_U_DATA_N<2>
74 73 LVDS_U_DATA_P<2>
74 73 LVDS_U_CLK_N
74 73 LVDS_U_CLK_P

C9421 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD4

INVERTER INTERFACE

62 =PPBUS_S0_INVERTER

L9450 FERR-1K-OHM-EMI SM

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

62 =PP5V_S0_INVERTER

Q9450 FDG6324L SC70-6-LF

R9450 100K 5% 1/16W MF-LF 402

FP_PWR_EN_L

L9452 400-OHM-EMI SM-1

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9451 10UF 20% 6.3V X5R 603

CRITICAL
J9450 SM-2MT-LF

NC 5

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

NC 6

INVERTER_PWM

GND_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

L9454 400-OHM-EMI SM-1

C9454 0.001uF 20% 50V CERM 402

C9455 0.001uF 20% 50V CERM 402

L9455 FERR-250-OHM SM

LCD_CTL_SMC
R9490 0 5% 1/16W MF-LF 402

46 SMC_BKLIGHT_ENABLE

LCD_CTL_GPU
R9491 0 5% 1/16W MF-LF 402

69 GPU_BLON

GPU_OR_SMC_BL_EN

R9489 10K 5% 1/16W MF-LF 402

62 =PP3V3_S0_INVERTER

INVERTER_BUF

U9453 MC74VHC1G08 SC70

INVERTER_PWM_F

6 =GND_CHASSIS_INVERTER

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

LCD_CTL_SMC
R9492 0 5% 1/16W MF-LF 402

46 SMC_DISP_BKLT_A

GPU_OR_SMC_BL_PWM

INVERTER_BUF

C9453 0.1uF 20% 25V CERM 402

LCD_CTL_GPU
R9493 0 5% 1/16W MF-LF 402

72 GPU_VARY_BL

INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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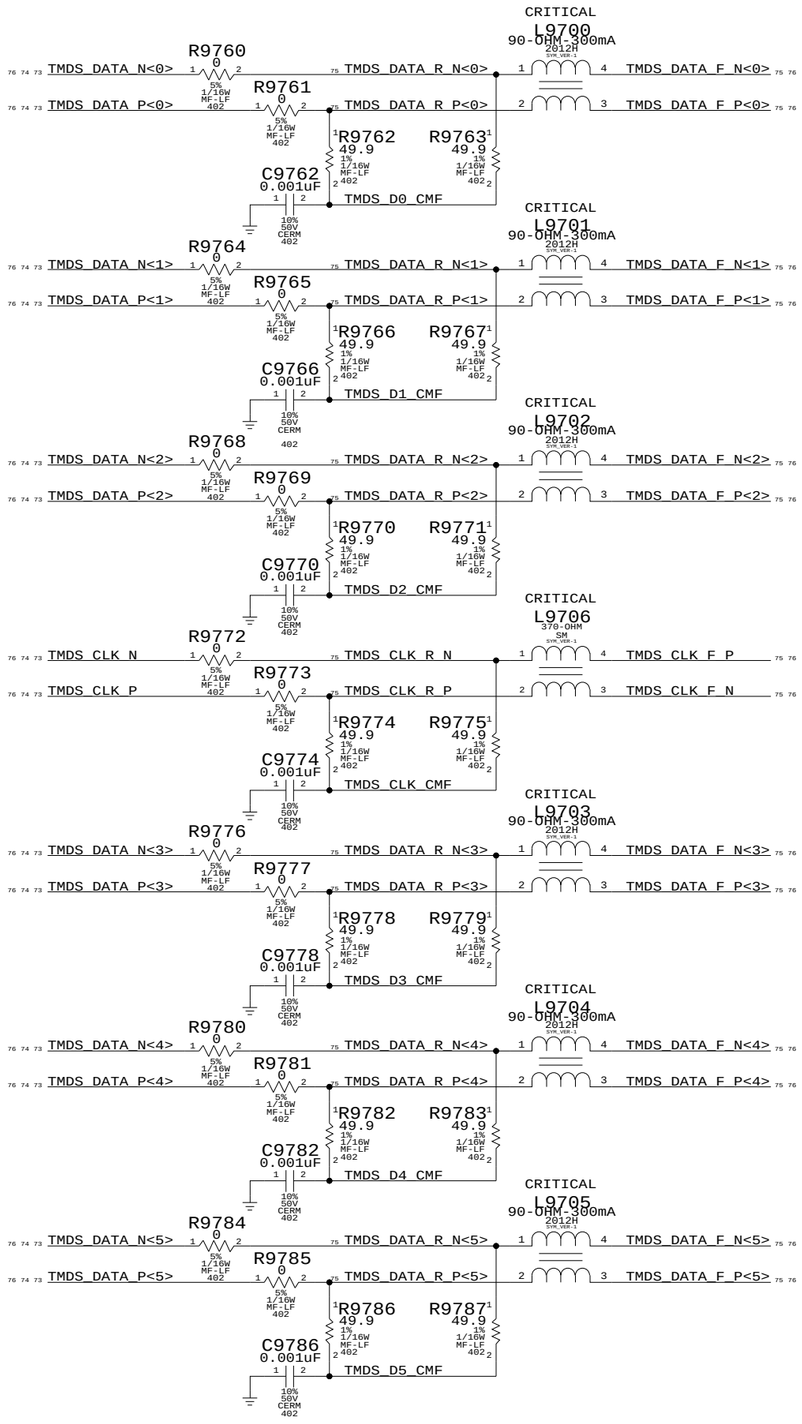
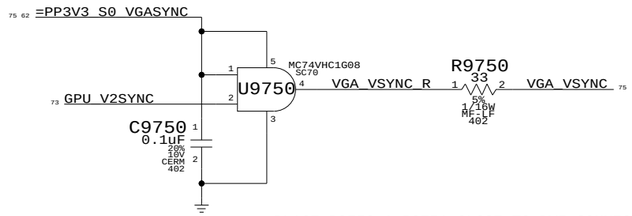
TMDS Filtering

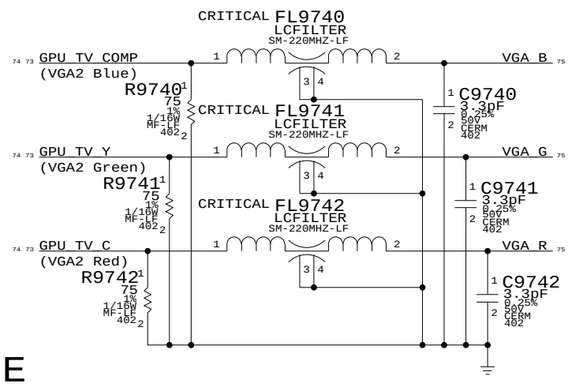
Place series R's close to GPU, other parts near connector.



VGA SYNC BUFFERS

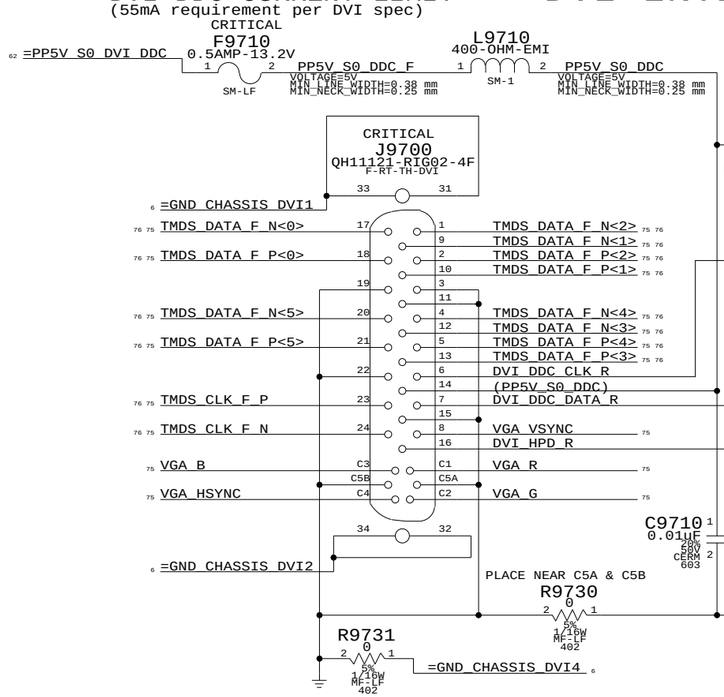


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDSCONN_CLK_F_P
	TMDSCONN	TMDSCONN_CLK_F_N
	TMDSCONN	TMDSCONN_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN_DATA_F_N<5..0>

External Display Connector

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
LV0	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
LV1	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
LV2	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
LV3	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

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